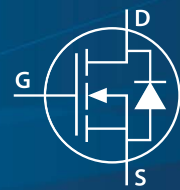
EPC2305 – Enhancement Mode Power Transistor

V_{DS} , 150 V
$R_{DS(on)}$, 2.2 mΩ typ

Preliminary



EFFICIENT POWER CONVERSION

RoHS Halogen-Free

General Description

The EPC2305 is a 150 V eGaN® power transistor in a low inductance 3 x 5 mm QFN package with exposed top for excellent thermal management.

The thermal resistance to case top is ~0.2 °C/W, resulting in excellent thermal behavior and easy cooling. The device features an enhanced PQFN "Thermal-Max" package. The exposed top enhances top-side thermal management and the side-wettable flanks guarantee that the complete side-pad surface is wetted with solder during the reflow soldering process, which protects the copper and allows soldering to occur on this external flank area for easy optical inspection.

Compared to a Si MOSFET, the footprint of 15 mm^2 is less than half of the size of the best-in-class Si MOSFET with similar $R_{DS(on)}$ and voltage rating, Q_G and Q_{GD} are significantly smaller and Q_{RR} is 0. This results in lower switching losses and lower gate driver losses. In summary, EPC2305 allows the highest power density due to enhanced efficiency, smaller size, and higher switching frequency for smaller inductor and fewer capacitors.

The EPC2305 enables designers to improve efficiency and save space. The excellent thermal behavior enables easier and lower cost cooling. The ultra-low capacitance and zero reverse recovery of the eGaN® FET enables efficient operation in many topologies. Performance is further enhanced due to the small, low inductance footprint.

Application Notes:

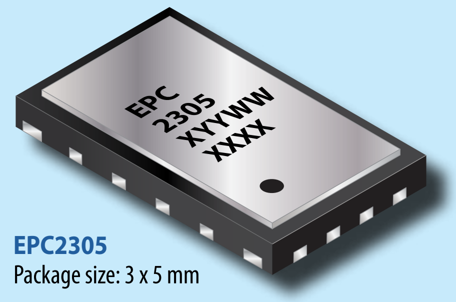
- Easy-to-use and reliable gate, Gate Drive ON = 5 V typical, OFF = 0 V (negative voltage not needed)
- Top of FET is electrically connected to source

Questions:

ASK AN EXPERT GaN

Maximum Ratings

	PARAMETER	VALUE	UNIT
V_{DS}	Drain-to-Source Voltage (Continuous)	150	V
	Drain-to-Source Voltage (up to 10,000 5 ms pulses at 150 °C)	180	
I_D	Continuous (T_A = 25°C)	102	A
	Pulsed (25°C, T_{PULSE} = 300 µs)	329	
V_{GS}	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-4	
T_J	Operating Temperature	–40 to 150	°C
T_{STG}	Storage Temperature	–40 to 150	



EPC2305
Package size: 3 x 5 mm

Features

- 150 V
- 2.2 mΩ typical
- 3 x 5 mm QFN Package

Applications

- High frequency DC/DC
- AC/DC Chargers and Adaptors
- BLDC Motor Drive
- eMobility Motor drives
- Solar Optimizer & MPPT
- Synchronous Rectification for chargers, adaptors, power supplies
- Class D Audio
- Fast charging for phone & notebook, gaming PC
- DC/DC and chargers for eMobility, power tools, vacuum cleaners

Benefits

- Ultra High Efficiency
- No Reverse Recovery
- Ultra Low Q_G
- Small Footprint
- Excellent Thermal

Scan QR code or click link below for more information including reliability reports, device models, demo boards!

https://l.ead.me/EPC2305

Thermal Characteristics			
PARAMETER		TYP	UNIT
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Case TOP)	0.2	°C/W
$R_{\theta JB}$	Thermal Resistance, Junction-to-Board (Case BOTTOM)	1.5	
$R_{\theta JA\_JEDEC}$	Thermal Resistance, Junction-to-Ambient (using JEDEC 51-2 PCB)	45	
$R_{\theta JA\_EVB}$	Thermal Resistance, Junction-to-Ambient (using EPC90142 EVB)	21	

Static Characteristics (T_J = 25°C unless otherwise stated)						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 V, I_D = TBD mA	150			V
I_{DSS}	Drain-Source Leakage	V_{DS} = 120 V, V_{GS} = 0 V		0.002		mA
I_{GSS}	Gate-to-Source Forward Leakage	V_{GS} = 5 V		0.016		
	Gate-to-Source Forward Leakage#	V_{GS} = 5 V, T_J = 125°C		0.7		
	Gate-to-Source Reverse Leakage	V_{GS} = -4 V		0.006		
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 11 mA	0.7	1.1	2.5	V
$R_{DS(on)}$	Drain-Source On Resistance	V_{GS} = 5 V, I_D = 30 A		2.2		mΩ
V_{SD}	Source-to-Drain Forward Voltage#	I_S = 0.5 A, V_{GS} = 0 V		1.4		V

Defined by design. Not subject to production test.

Dynamic Characteristics# (T_J = 25°C unless otherwise stated)						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{ISS}	Input Capacitance	V_{DS} = 75 V, V_{GS} = 0 V		2900		pF
C_{RSS}	Reverse Transfer Capacitance			7		
C_{OSS}	Output Capacitance			920		
$C_{OSS(ER)}$	Effective Output Capacitance, Energy Related (Note 1)	V_{DS} = 0 to 75 V, V_{GS} = 0 V		1100		
$C_{OSS(TR)}$	Effective Output Capacitance, Time Related (Note 2)			1400		
R_G	Gate Resistance			0.5		Ω
Q_G	Total Gate Charge	V_{DS} = 75 V, V_{GS} = 5 V, I_D = 30 A		21		nC
Q_{GS}	Gate-to-Source Charge	V_{DS} = 75 V, I_D = 30 A		6.3		
Q_{GD}	Gate-to-Drain Charge			2.6		
$Q_{G(TH)}$	Gate Charge at Threshold			4.4		
Q_{OSS}	Output Charge	V_{DS} = 75 V, V_{GS} = 0 V		105		
Q_{RR}	Source-Drain Recovery Charge			0		

Defined by design. Not subject to production test.
All measurements were done with substrate shorted to source.
Note 1: $C_{OSS(ER)}$ is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS}.
Note 2: $C_{OSS(TR)}$ is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS}.

Figure 1: Typical Output Characteristics at 25°C

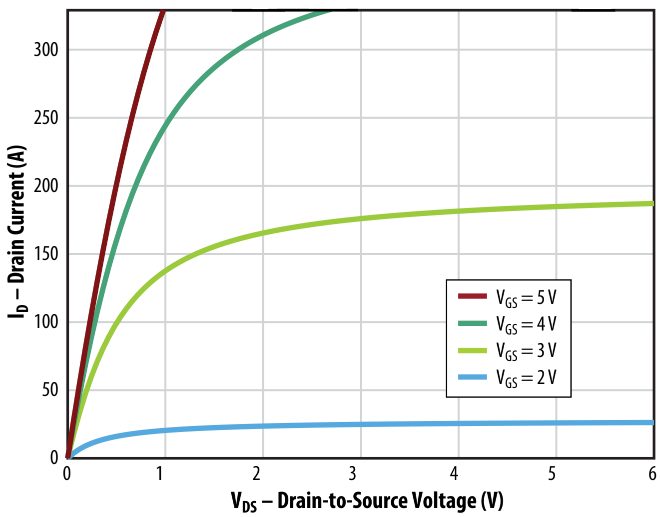


Figure 2: Typical Transfer Characteristics

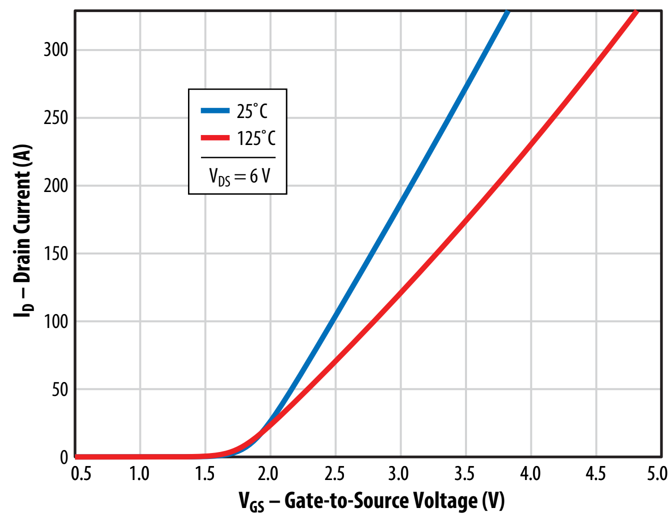


Figure 3: Typical $R_{DS(on)}$ vs. V_{GS} for Various Drain Currents

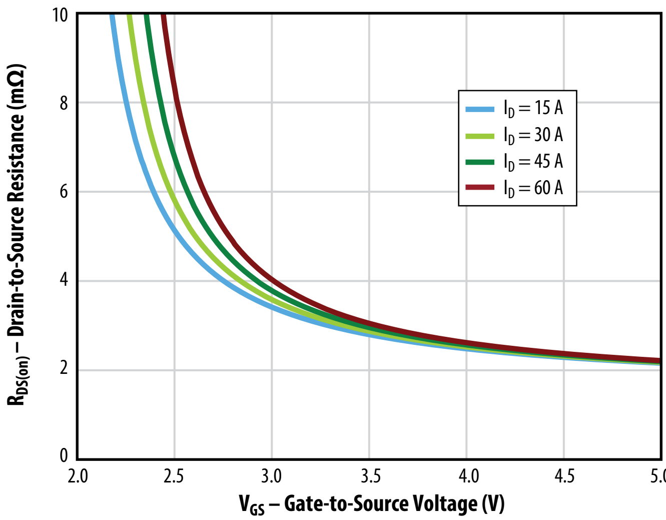


Figure 4: Typical $R_{DS(on)}$ vs. V_{GS} for Various Temperatures

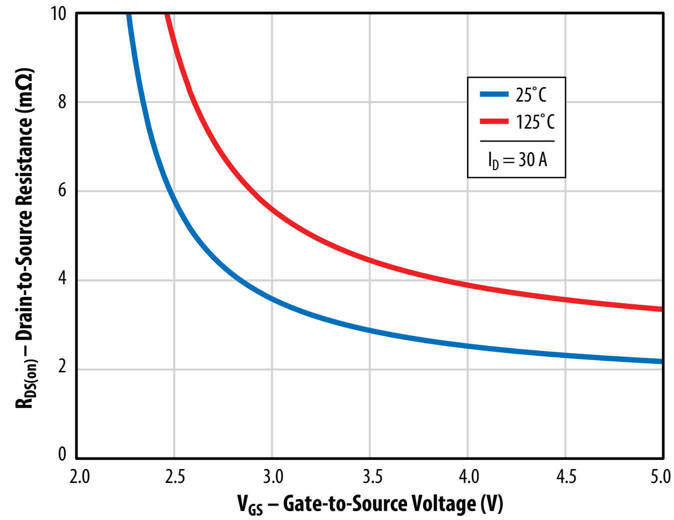


Figure 5a: Typical Capacitance (Linear Scale)

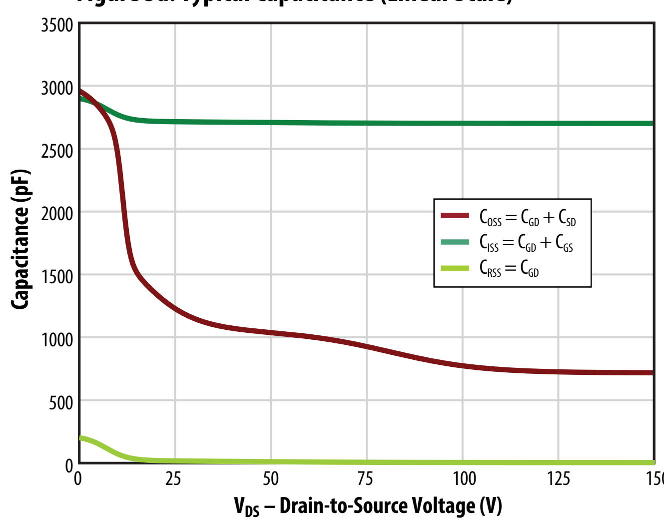


Figure 5b: Typical Capacitance (Log Scale)

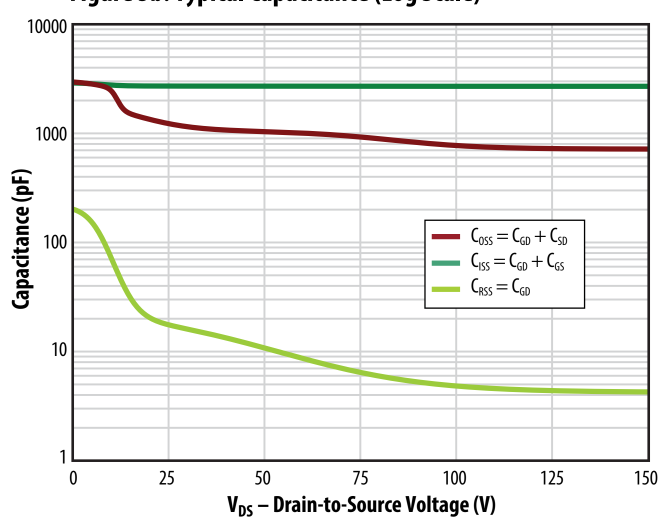


Figure 6: Typical Output Charge and C_{OSS} Stored Energy

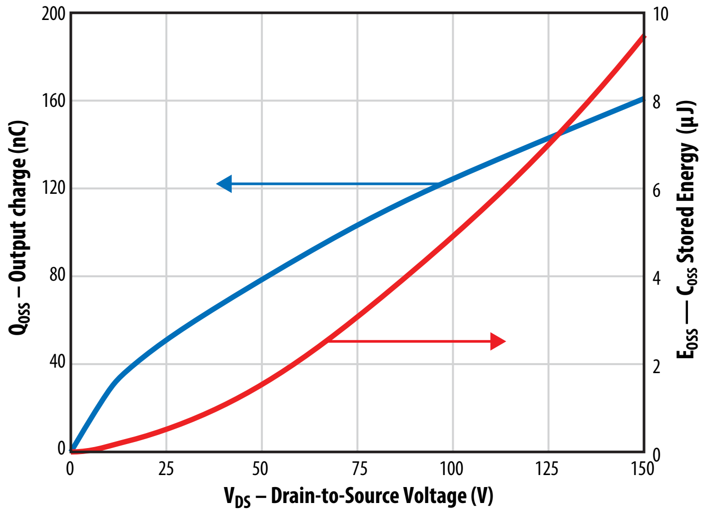


Figure 7: Typical Gate Charge

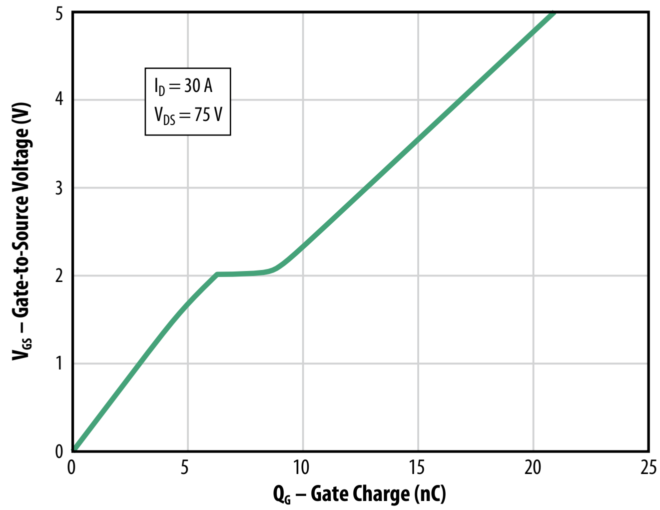
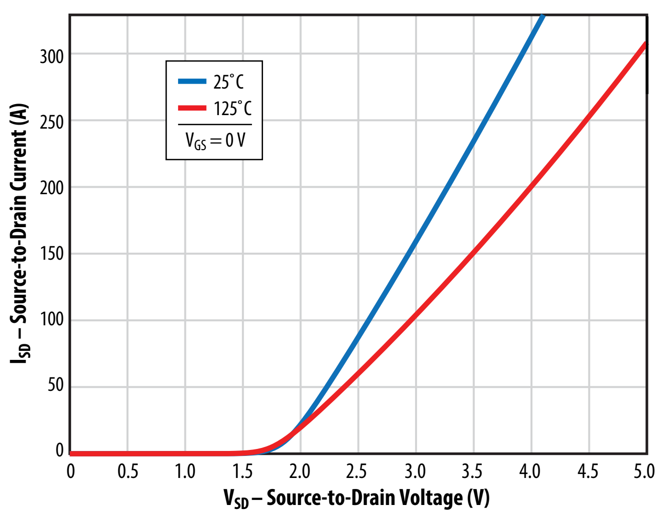


Figure 8: Typical Reverse Drain-Source Characteristics



Negative gate drive voltage increases the reverse drain-source voltage.
EPC recommends 0 V for OFF

Figure 9: Typical Normalized On-State Resistance vs. Temp.

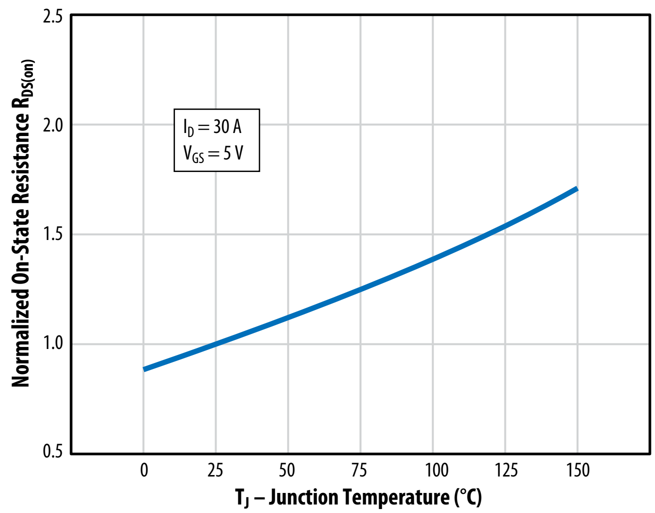


Figure 10: Typical Normalized Threshold Voltage vs. Temp.

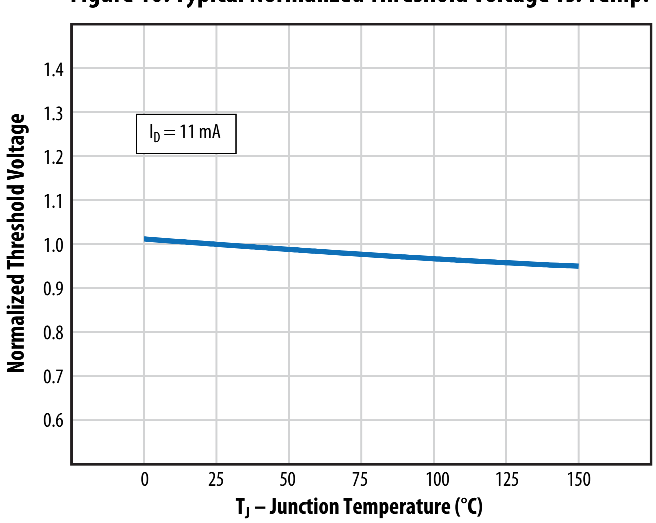


Figure 11: Safe Operating Area

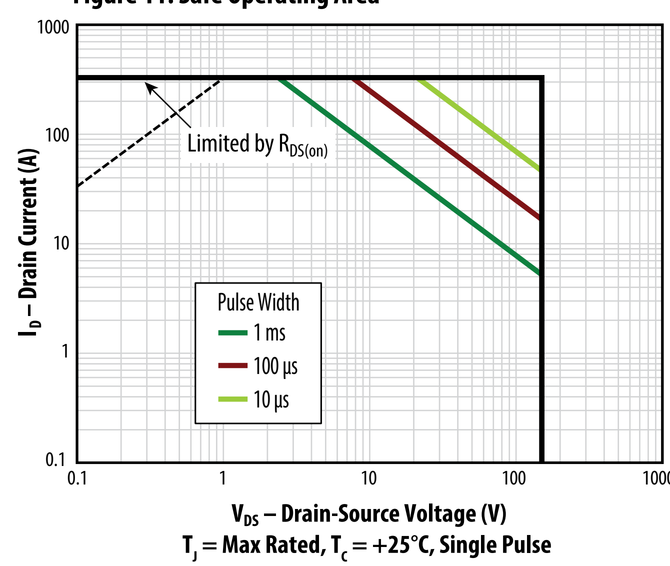
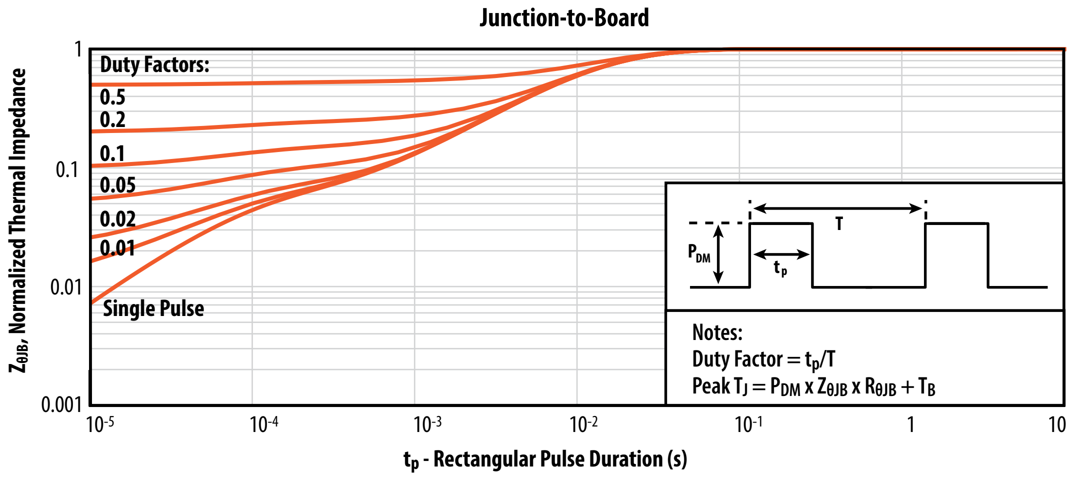
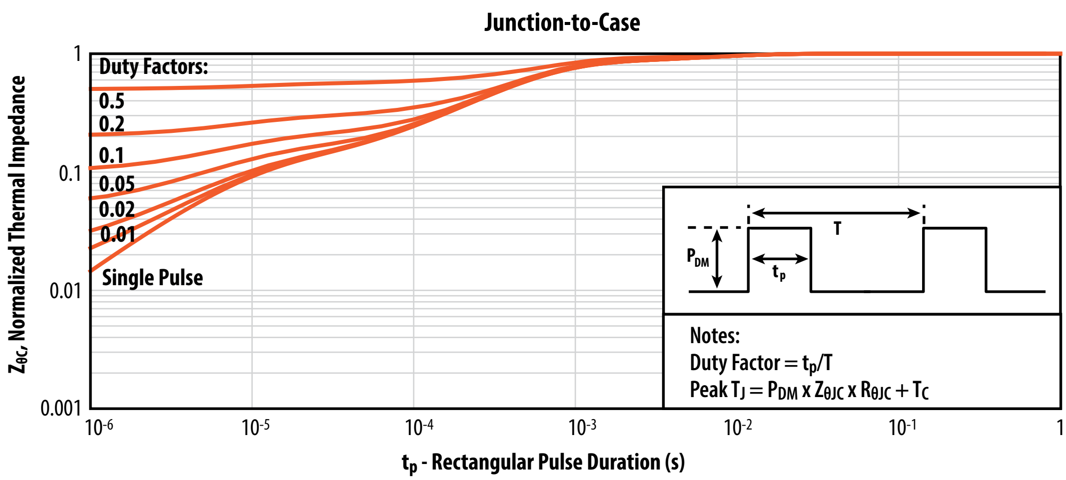
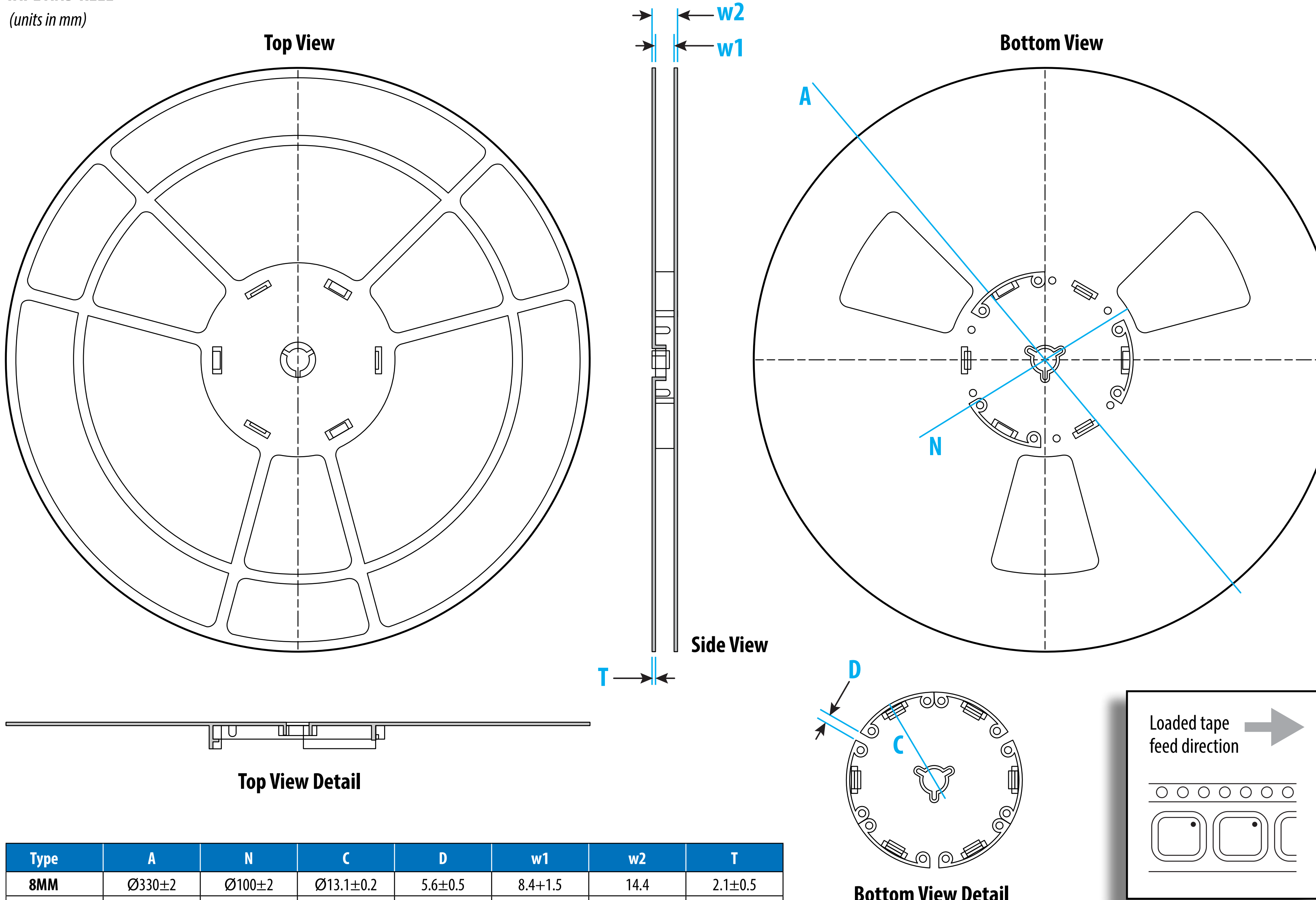


Figure 12: Transient Thermal Response Curves

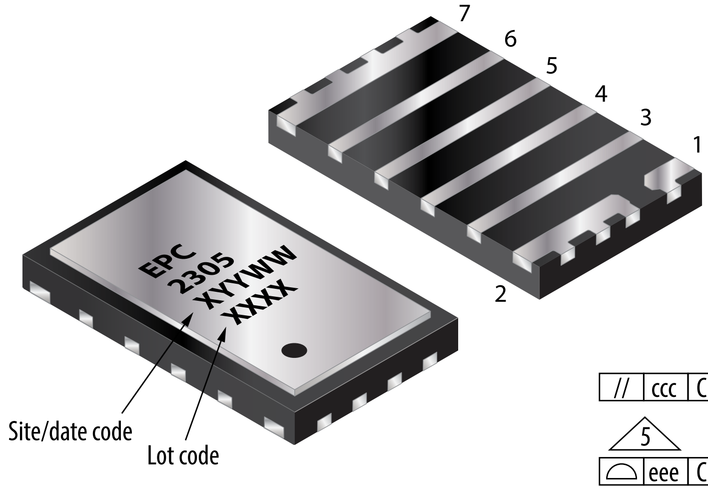


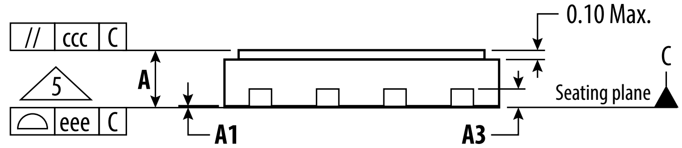


TAPE AND REEL
(units in mm)

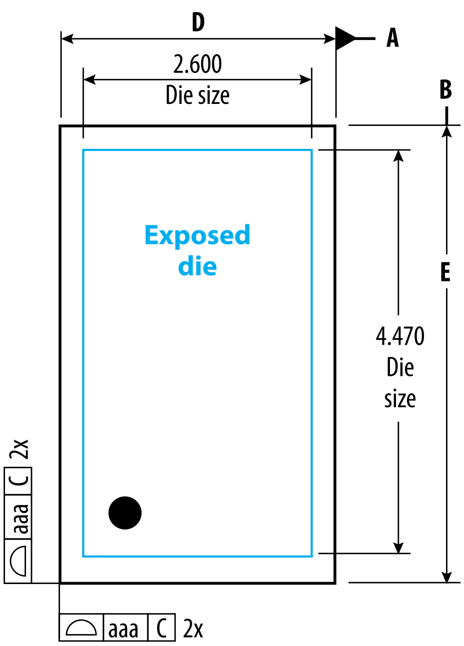


Type	A	N	C	D	w1	w2	T
8MM	Ø330±2	Ø100±2	Ø13.1±0.2	5.6±0.5	8.4+1.5	14.4	2.1±0.5
12MM	Ø330±2	Ø100±2	Ø13.1±0.2	5.6±0.5	12.4+1.5	18.4	2.1±0.5
16MM	Ø330±2	Ø100±2	Ø13.1±0.2	5.6±0.5	16.4+1.5	22.4	2.1±0.5
24MM	Ø330±2	Ø100±2	Ø13.1±0.2	5.6±0.5	24.4+1.5	30,4	2.1±0.5

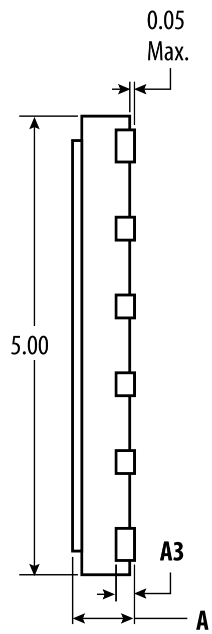




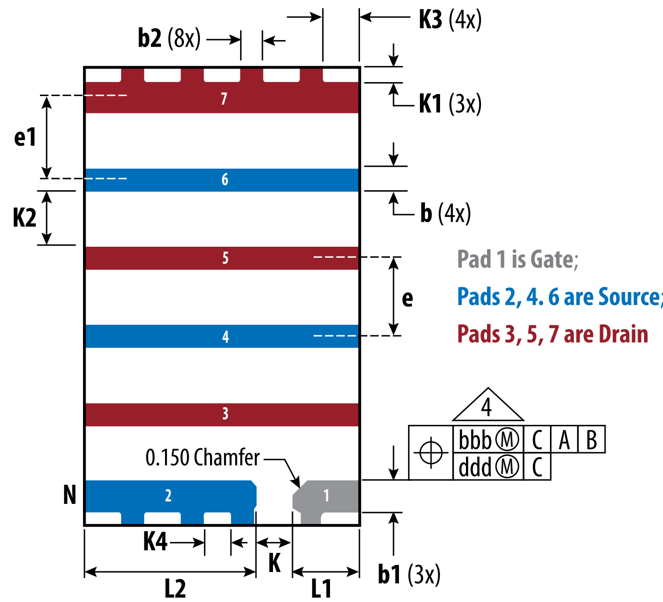
Side View 2



Top View



Side View 1



Bottom View

SYMBOL	Dimension (mm)			
	MIN	Nominal	MAX	Note
A	0.60	0.65	0.70	
A1	0.00	0.02	0.05	
A3		0.20 Ref		
b	0.20	0.25	0.30	4
b1	0.30	0.35	0.40	4
b2	0.20	0.25	0.30	4
D		3.00 BSC		
E		5.00 BSC		
e		0.85 BSC		
e1		0.90 BSC		
L1	0.625	0.725	0.825	
L2	1.775	1.875	1.975	

SYMBOL	Dimension (mm)			
	MIN	Nominal	MAX	Note
K	0.35	0.40	0.45	
K1	0.10	0.15	0.20	
K2	0.55	0.60	0.65	
K3	0.35	0.40	0.45	
K4	0.25	0.30	0.35	
aaa		0.05		
bbb		0.10		
ccc		0.10		
ddd		0.05		
eee		0.08		
N		15		3
NE		6		

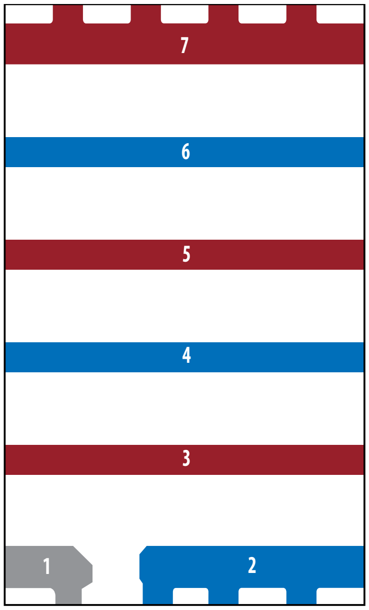
Notes:

1. Dimensioning and tolerancing conform to ASME Y14.5-2009
2. All dimensions are in millimeters
3. **N** is the total number of terminals

△4. Dimension **b** applies to the metallized terminal. If the terminal has a radius on the other end of it, dimension **b** should not be measured in that radius area.

△5. Coplanarity applies to the terminals and all the other bottom surface metallization.

TRANSPARENT VIEW

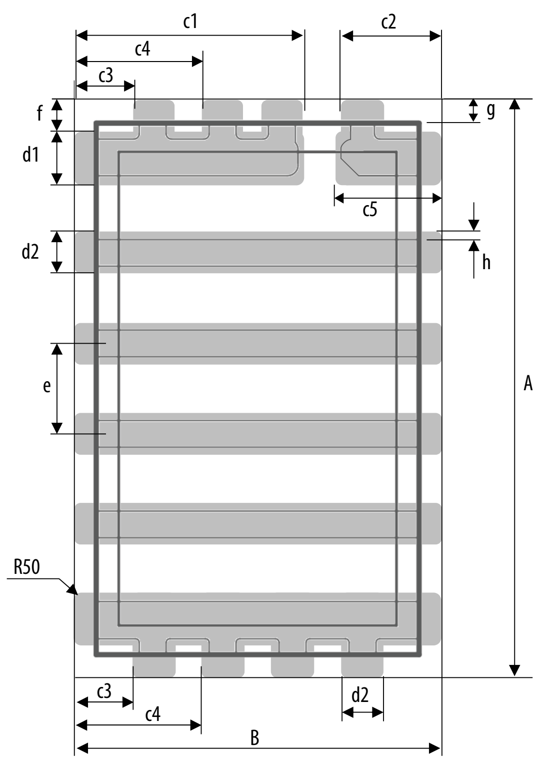


Transparent Top View

PIN	DESCRIPTION
1	Gate
2	Source
3	Drain
4	Source
5	Drain
6	Source
7	Drain

RECOMMENDED LAND PATTERN

(units in mm)



Land pattern is solder mask defined.

DIM	Nominal
A	5.4
B	3.4
c1	2.11
c2	0.90
c3	0.55
c4	1.20
c5	0.975
d1	0.45
d2	0.35
e	0.85
f	0.30
g	0.2
h	0.05

Additional resources available:

- Assembly resources – https://epc-co.com/epc/Portals/0/epc/documents/product-training/Appnote_GaNassembly.pdf
- Library of Altium footprints for production FETs and ICs – https://epc-co.com/epc/documents/altium-files/EPC%20Altium%20Library.zip (for preliminary device Altium footprints, contact EPC)