IN612L Datasheet

IN612L

Bluetooth 5 & Software Defined Radio Wireless SoC

Key Features

- **Multi-mode collaborative protocol stack**
  - Bluetooth 5
    - Bluetooth 5 spec fully compliant
    - High Data Rate supports up to 2Mbps
    - Long Range support (125Kbps/500Kbps)
    - Advertising Extension support
  - SDR (Software defined radio, user defined)
    - Flexible Rx/Tx enable control
    - Event triggering mode for low power design
    - True Bi-directional
    - Concurrent with Bluetooth 5 operation

- **CPU & memory**
  - ARM Cortex-M4F up to 64MHz with 16KB i-cache
  - 256KB ROM (bootloader & SW stack)
  - Up to 96KB user SRAM
  - 4Kb eFuse memory (Manufacturer ID, Security Key storage)
  - 512KB Flash memory (Stacked, XIP mode support)
  - Over-The-Air Update (OTA) support
  - SWD/JTAG debug interface

- **Radio**
  - 2.4GHz transceiver, Bluetooth 5 compliant
  - Rx sensitivity –104.5 dBm @ 125Kbps
  - Rx sensitivity –97.5 dBm @ 1Mbps
  - Rx sensitivity –94.5 dBm @ 2Mbps
  - Tx output 0dBm, 4.1mA, up to +3 dBm
  - Rx 5mA
  - Link budget of 107.5 dB @ 125Kbps
  - MedRadio Band Support (2360MHz~2400MHz)

- **Peripheral**
  - Up to 30 GPIOs
  - 2 I2C, master/slave up to 1000kHz clock
  - 1 SPI master w/ up to 4 SPI slaves supported, up to 16MHz clock
  - 1 SPI slave, up to 8MHz
  - 2 UART up to 2MHz
  - 5 dedicated PWMs, up to 13 PWM through I/O configuration
  - 1 I2S master and 1 I2S slave, bi-directional stereo support
  - 2 PDM mono or 1 stereo with clock range from 160kHz – 5.12MHz
  - ISO7816
  - Keyboard scanner – up to 14x14 matrix
  - QDEC
  - 11-bit ADC, up to up to 64 KSPS, up to 11 channels
  - 8 counters/timers

- **Clock sources**
  - 32MHz crystal, 32.768 kHz RTC

- **DMA Controller**
  - Up to 2 concurrent DMA streams with 2 channels each

- **Voice/Audio engine**
  - Build-in stereo/mono ADPCM codec with 4:1 compression
  - Support both ADPCM and raw PCM as output with sampling frequency up to 64kHz
  - PDM or I2S as input
  - Sigma-delta audio DAC output

- **Security**
  - HW ECC, AES256, SHA-1, SHA-2
  - Secure Boot, Software copyright protection
  - True Random Number Generator (FIPS140-2 compliant)

- **Power mode**
  - Deep Sleep mode 500nA with 32kHz RC ON
  - Shutdown mode <20nA

- **PMU**
  - Integrated DCDC buck convertor
  - 1.7 - 3.6V input

- **Packaging**
  - QFN48 6x6mm

- **Operating temperature**
  - -40 ~ +85 °C

- **Typical applications**
  - IoT applications
  - Bluetooth Gateway
  - Smart home automation, Smart Lighting
  - Industrial IoT
  - Wearables, toys,
  - Asset tracking management
  - Smart retail applications
  - Connected appliances, locks

About Documentation

Document name	Datasheet	
Part number	IN612L, IN610L, IN610	
Control number	IN6IDOC-DS-IN612L-EN-V1_1.10	For external use
Revision	V1.10	

Product status	Document content	Data status
In development	Objective Specification/MRD	Target Specification. Revised and supplementary data will be published later
Engineering sample	Specification with measured data on E/S	Data based on early E/S sample testing
Customer sample	Specification with measured data on the early production samples	Data based on early production samples. Revised and supplementary data may be published later.
Mass production		Document contains final product specification

This document applies to the following products:

Product name	Part number	Product status
IN612L	IN612L-Q1-R-G4C0I	Mass production
IN610L	IN610L-Q1-R-G4C0I	Mass Production
IN610	IN610-Q1-R-G4C0I	Mass Production

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1. Product Overview

IN612L is one of InPlay's SwiftRadio™ SoC product family which features multi-mode collaborative protocol stack with 2.4Ghz frequency band RF radio and MCU system integrated. The product integrates developer friendly Software Defined Radio and Bluetooth 5 with full specification compliant such as 2Mbps high data rate mode, 125Kbps/500Kbps Coded PHY rate support as well as the extended advertising capabilities. The user defined SDR stack and its built-in Bluetooth 5 stack can be operated concurrently so that many complicated networking application challenges can be well addressed and optimized.

The device integrates a powerful 32bit ARM Cortex-M4F CPU with floating point unit processing capability. It has built-in 256KB ROM, 512KB Flash memory and high density up to 96KB SRAM which can be used as user data space for sophisticated algorithms and applications.

The device has an excellent RF performance with ultra-low power consumption design philosophy in mind, so it is well suited for power constraint applications such as battery powered products (ex. retail beacon and wearables). Along with the powerful ARM Coretex-M4F CPU and rich memory resources integrated into the device, user can develop as many applications without adding additional CPU.

The device has well-crafted hardware security engine designed which supports AES128, AES256, SHA-1, SHA-2 and ECC encryption and decryption algorithms. It also has True Random Number Generator (TRNG) integrated to facilitate security application implementation. The security engine includes two independent sets of crypto engines which to serve not only the Bluetooth 5 radio link layer enhanced security but also user application security requirement.

In addition to the sophisticated design on radio and communication modems, the device integrates variety of peripherals such as I2C, SPI, UART, PDM and I2S for user applications. IN612L comes with package option of QFN48.

The *Figure 1* below shows the system block diagram of SwiftRadio™ SoC IN6xx product family. And features available on the diagram will vary by part number. For more information on available features of different devices, please refer to Ordering Information.

In the InPlay's SwiftRadio™ SoC product family. There are three products:IN612L, IN610L, and IN610. The three products support the same feature set except those listed in *Table 1* .

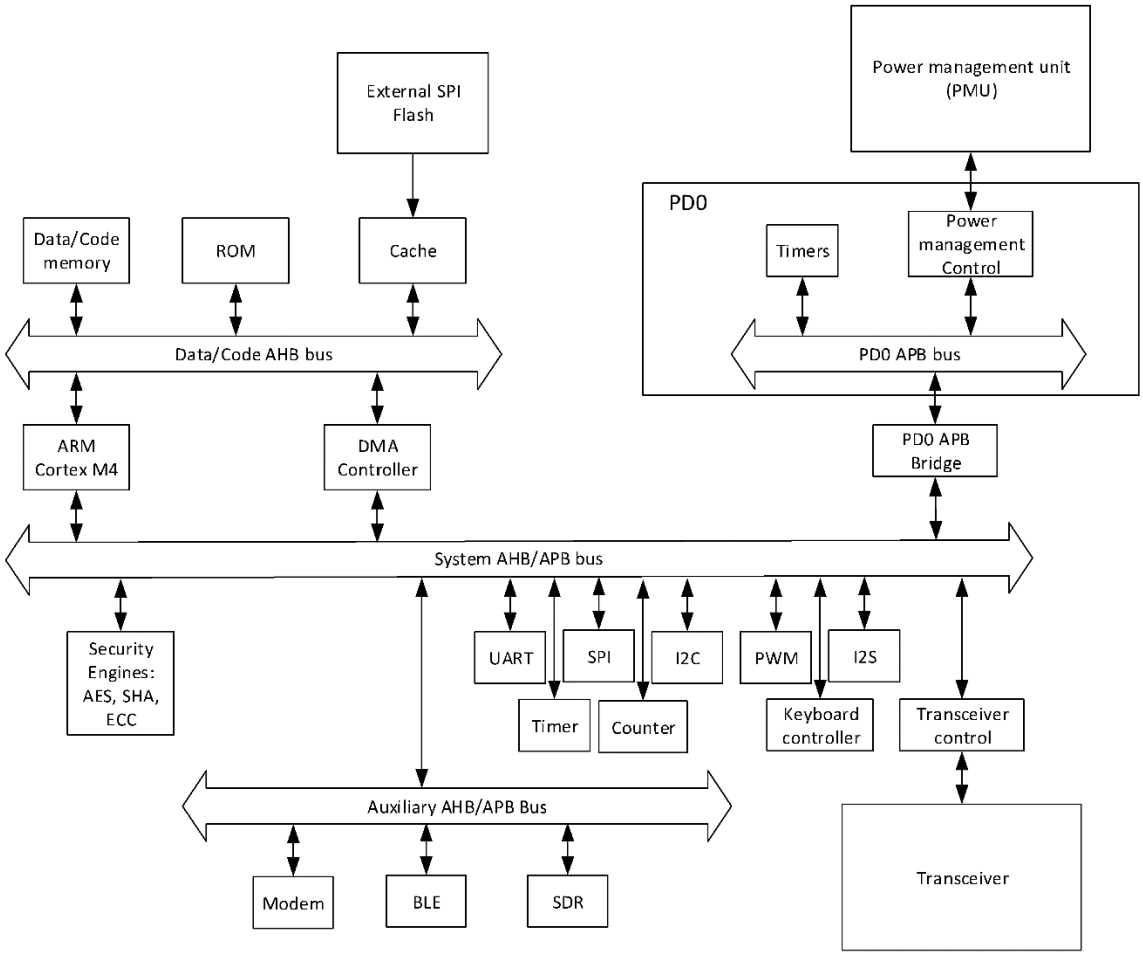


Figure 1： Device system block diagram

Table 1 : Products and feature difference

Feature	Product		
	IN612L	IN610L	IN610
Soft defined radio (SDR)	Supported	Not supported	Not supported
Coded BLE PHY rate (125K,500K)	Supported	Supported	Not supported

2. Pin Map Information

2.1. QFN48

IN612L is offered in an exposed pad 48 pin QFN package. This package has an exposed paddle that must be connected to the system board ground. In *Figure 2* , the QFN package pin assignment is shown.

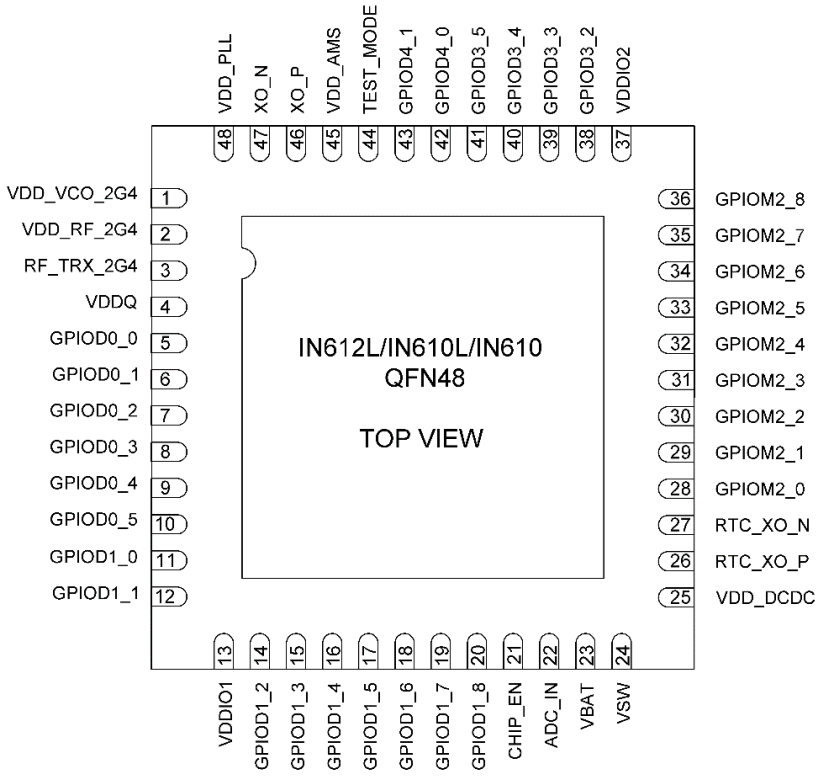


Figure 2：IN612L/IN610L/IN610 pin assignment of QFN48

Table 2：IN612L/IN610L/IN610 QFN48 pin description

Pin #	Pin name	Pin type	Description
1	VDD_VCO_2G4	Analog/RF	RF VCO power supply 1.2V
2	VDD_RF_2G4	Analog/RF	RF power supply 1.2V
3	RF_TRX_2G4	Analog/RF	RF port
4	VDDQ	Power Supply	eFuse programming voltage supply 3.3V
5	GPIOD_0_0	Digital I/O	Digital signal GPIO_0_0
6	GPIOD_0_1	Digital I/O	Digital signal GPIO_0_1
7	GPIOD_0_2	Digital I/O	Digital signal GPIO_0_2

Pin #	Pin name	Pin type	Description
8	GPIOD_0_3	Digital I/O	Digital signal GPIO_0_3
9	GPIOD_0_4	Digital I/O	Digital signal GPIO_0_4
10	GPIOD_0_5	Digital I/O	Digital signal GPIO_0_5
11	GPIOD_1_0	Digital I/O	Digital signal GPIO_1_0
12	GPIOD_1_1	Digital I/O	Digital signal GPIO_1_1
13	VDDIO1	I/O Power	I/O voltage supply for GPIO power domain 1
14	GPIOD_1_2	Digital I/O	Digital signal GPIO_1_2
15	GPIOD_1_3	Digital I/O	Digital signal GPIO_1_3
16	GPIOD_1_4	Digital I/O	Digital signal GPIO_1_4
17	GPIOD_1_5	Digital I/O	Digital signal GPIO_1_5
18	GPIOD_1_6	Digital I/O	Digital signal GPIO_1_6
19	GPIOD_1_7	Digital I/O	Digital signal GPIO_1_7
20	GPIOD_1_8	Digital I/O	Digital signal GPIO_1_8
21	CHIP_EN	PMU	Chip enable
22	ADC_IN	PMU	Sensor ADC input
23	VBAT	PMU	Chip power supply
24	VSW	PMU	DCDC converter switching node
25	VDD_DCDC	PMU	DCDC converter Feedback node
26	RTC_XO_P	PMU	RTC positive terminal
27	RTC_XO_N	PMU	RTC negative terminal
28	GPIOM_2_0	Mixed signal I/O	Mixed signal GPIO_2_0
29	GPIOM_2_1	Mixed signal I/O	Mixed signal GPIO_2_1
30	GPIOM_2_2	Mixed signal I/O	Mixed signal GPIO_2_2
31	GPIOM_2_3	Mixed signal I/O	Mixed signal GPIO_2_3
32	GPIOM_2_4	Mixed signal I/O	Mixed signal GPIO_2_4
33	GPIOM_2_5	Mixed signal I/O	Mixed signal GPIO_2_5
34	GPIOM_2_6	Mixed signal I/O	Mixed signal GPIO_2_6
35	GPIOM_2_7	Mixed signal I/O	Mixed signal GPIO_2_7
36	GPIOM_2_8	Mixed signal I/O	Mixed signal GPIO_2_8
37	VDDIO2	I/O power	I/O voltage supply for GPIO power domain 2
38	GPIOD_3_2	Digital I/O	Digital signal GPIO_3_2
39	GPIOD_3_3	Digital I/O	Digital signal GPIO_3_3
40	GPIOD_3_4	Digital I/O	Digital signal GPIO_3_4
41	GPIOD_3_5	Digital I/O	Digital signal GPIO_3_5

Pin #	Pin name	Pin type	Description
42	GPIOD_4_0	Digital I/O	Digital signal GPIO_4_0
43	GPIOD_4_1	Digital I/O	Digital signal GPIO_4_1
44	TEST_MODE	Digital input	Test mode selection, GND for normal operation
45	VDD_AMS	Analog/RF	AMS Supply 1.2V
46	XO_P	Analog/RF	XO positive terminal
47	XO_N	Analog/RF	XO negative terminal
48	VDD_PLL	Analog/RF	RF PLL Power Supply 1.2V

Table 3 shows the Pin Mux configuration that developers can use to configure the I/O functionality based on application needs. Only one Pin Mux option can be chosen and once configured, the chip I/O functionality will be fixed based on the configuration.

Table 3 ： GPIO pin mux

Pin #	Pin name	Mux 1	Mux 2	Mux3	Mux4	Mux5	Mux6
5	GPIO_0_0	Uart_1_rts	Keyboard_0		I2c_0_scl		Pwm_0
6	GPIO_0_1		Keyboard_1	Spi_mstr_miso_bkup-1	I2c_0_sda		Pwm_1
7	GPIO_0_2	Uart_0_tx	Keyboard_25				Pwm_2
8	GPIO_0_3	Wlan_tx_bkup-0		Spi_mstr_mosi_bkup	I2c_1_scl	Audio_sd_l_bkup	Tx_en1
9	GPIO_0_4	Wlan_rx_bkup-0	Keyboard_4	Spi_mstr_clk_bkup	I2c_1_sda	Audio_sd_r_bkup	Tx_en1_bkup
10	GPIO_0_5		Keyboard_22				
11	GPIO_1_0	Uart_0_rx-1	Keyboard_24				i_swd_trace_clk-0
12	GPIO_1_1	Jtag_tms_swdio					
14	GPIO_1_2	Jtag_tcksck-1					
15	GPIO_1_3	Jtag_tdo	Keyboard_0_bkup	Qd_0_cha_x-0	I2s_mstr_clk	I2s_slv_clk-0	Swd_trace_swo
16	GPIO_1_4	Jtag_tdi-1	Keyboard_1_bkup	Qd_0_chb_x-0	I2s_mstr_ws	I2s_slv_ws	

Pin #	Pin name	Mux 1	Mux 2	Mux3	Mux4	Mux5	Mux6
17	GPIO_1_5	Uart_1_rts	Keyboard_2_bkup	Qd_0_idx_x-0	I2s_mstr_sd0	I2s_slv_sd0	Swd_trace_0
18	GPIO_1_6	Uart_1_cts-1	Keyboard_3	Qd_0_cha_y-0	I2s_mstr_sd1		Swd_trace_1
19	GPIO_1_7	Uart_1_tx	Keyboard_4_bkup	Qd_0_chb_y-0	I2c_0_scl_bkup	I2s_slv_sd0	Swd_trace_2
20	GPIO_1_8	Uart_1_rx-1	Keyboard_5_bkup	Qd_0_idx_y-0	I2c_0_sda_bkup	Pwm_4	Swd_trace_3
28	GPIO_2_0		Keyboard_5				
29	GPIO_2_1	Uart_1_tx_bkup	Keyboard_2	Spi_mstr_ssn0	Counter_0	Audio_sd_l	Tx_en_bkup
30	GPIO_2_2		Keyboard_19		Counter_1		
31	GPIO_2_3	Uart_0_tx_bkup		Qd_0_cha_z-0	Counter_2	Audio_sd_r	Rx_en_bkup
32	GPIO_2_4		Keyboard_18		Counter_3		
33	GPIO_2_5	Uart_0_rx_bkup-1	Keyboard_20	Qd_0_chb_z-0	Counter_4	32kHz_clk	Rx_en
34	GPIO_2_6				Counter_5		
35	GPIO_2_7	Uart_1_rx_bkup-1	Keyboard_23	Tv_infrd_out	Counter_6		Pdm_1_data-0
36	GPIO_2_8		Keyboard_3_bkup		Counter_7		Pdm_0_data-0
38	GPIO_3_2		Keyboard_27	Spi_mstr_ssn3	Wlan_tx-0		Wdt_reset
39	GPIO_3_3		Keyboard_26	Spi_mstr_ssn3	Wlan_rx-0		Wdt_reset_bkup
40	GPIO_3_4	Spi_mstr_clk		Spi_slv_clk-0	Ble_active	Qd_0_idx_z-0	Tx_en
41	GPIO_3_5	Spi_mstr_miso-1		Spi_slv_miso	Ble_active_bkup	Qd_0_led_x	32m_clk_out_bkup
42	GPIO_4_0	Spi_mstr_mosi	Keyboard_21	Spi_slv_mosi-1	I2c_1_scl_bkup	Qd_0_led_y	Pdm_0_clk
43	GPIO_4_1	Spi_mstr_ssn0		Spi_slv_ssn-1	I2c_1_sda_bkup	Qd_0_led_z	32m_clk_out
44	TEST_MODE						

3. Function Block Description

3.1. CPU and memory subsystem

The device integrates a powerful ARM Cortex-M4F processor core and their associated busses and memories. The Coretex-M4F processor incorporates a processor core, Nested Vectored Interrupt Controller (NVIC), high performance bus interfaces and a Floating-Point Unit (FPU).

The core processor has 16KB instruction cache. This subsystem also includes two independent DMA controllers with 4 channels each, 80KB of SRAM and 256KB of ROM. The subsystem integrates a hardwired cryptographic engine which is associated with the boot loader system to provide a secure boot implementation. This includes both system integrity check and authentication check of the application software. The advanced architecture design of system buses provides the exclusivity of access to radio communication blocks at the same time the flexibility of access to other peripheral blocks without sacrificing the system performance and stability. Active power consumption of the Cortex-M4F is 45uA/MHz at 3.3V as chip supply voltage with the built-in buck converter enabled and 1.2V as core supply voltage.

There are two DMA controllers with 2 channels each. They support independent accesses to peripherals using AHB bus to copy data from data/instruction memory to the peripheral memories or vice versa.

There is 96KB of SRAM memory, which can be fully retained or retained in increments of user defined blocks as small as 4KB. Among the 96KB of SRAM memory, 16KB can be used as cache memory for XIP (execute-in-place) flash memory controller.

There is 256KB of ROM memory that contains boot loader and Bluetooth 5 protocol stack. The device also integrates a 512KB or 1MB flash memory (part number dependent) for user program and data storage. The device supports XIP (execute-in-place) mode for the flash memory so that user can directly execute the program from flash memory rather than copying it into SRAM to run.

The device has integrated 4Kb of eFuse memory that can be used as security key storage and manufacture ID etc. Once the eFuse memory is being programmed and locked, the content of the memory will become permanent and cannot be modified or changed.

See *Figure 3* and *Figure 4* for the memory map in detail.

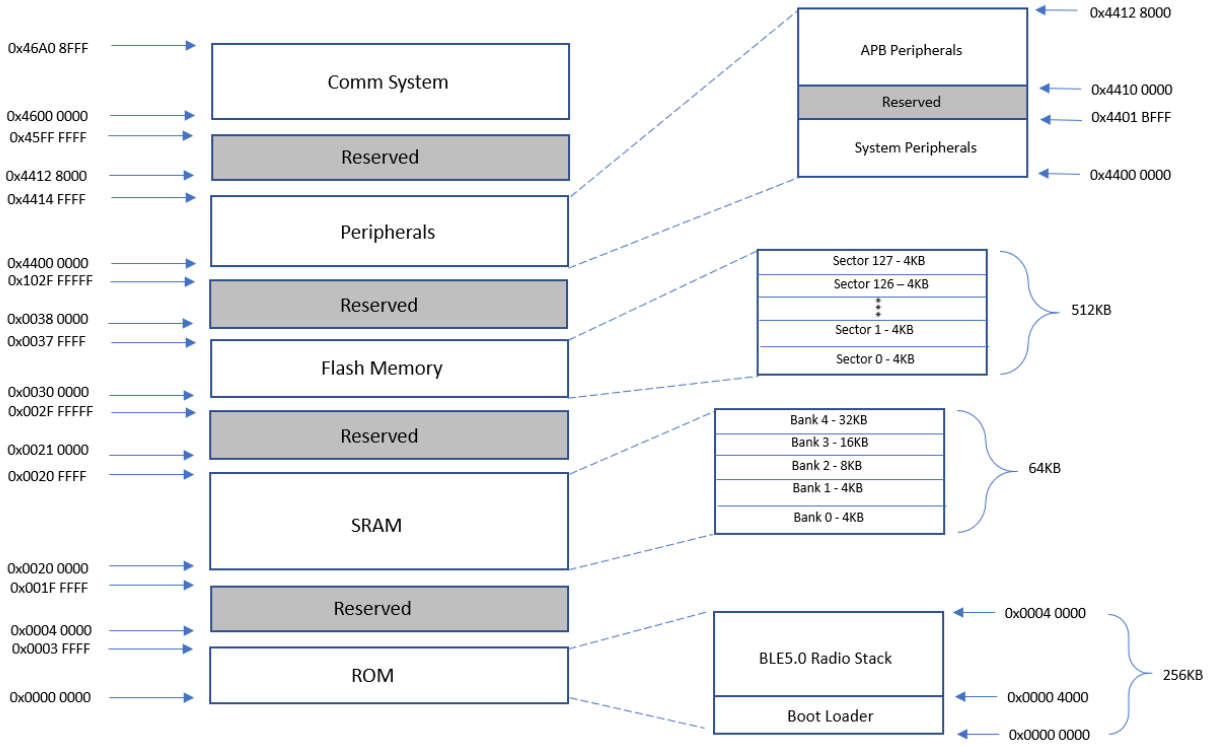


Figure 3 : Memory map

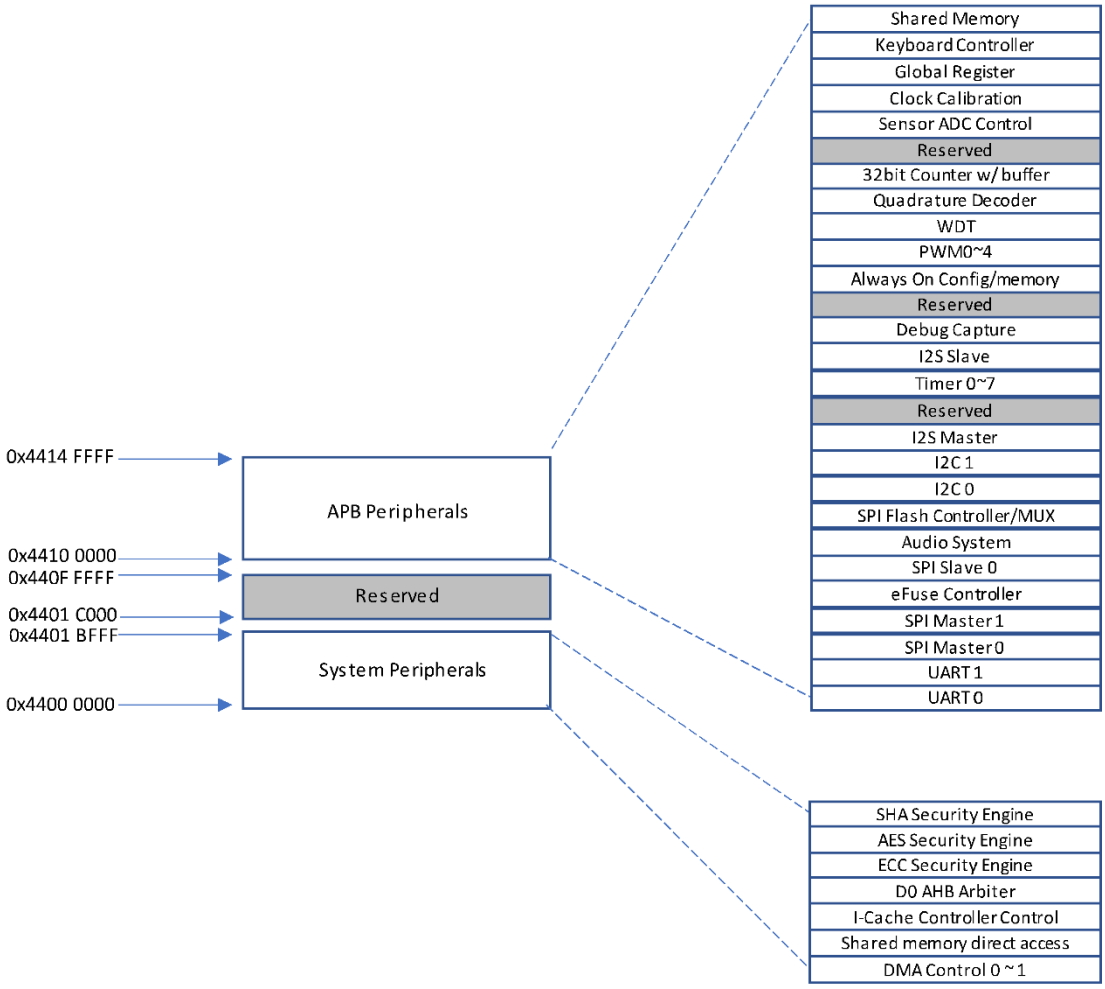


Figure 4 : Peripheral memory map

3.2. Power system and clocks

3.2.1. Power domains and power operation modes

The power supply system ensures the correct timing and voltage for each operating mode or block.

The device has the following power domains: AONPD (Always-On Power Domain), DOOPD (Dynamic On-Off Power Domain), and seven data/instruction memory banks, which can be in active, retention, or power-down mode.

Some power operation modes are listed as followings:

- Chip deep sleep mode. Only the AONPD domain is enabled. All other domains are closed. In this mode, the sleep timer is running, and the timer decides when to wake up the other domains. This mode can also be awakened by external wake-up pins or brownout detection trigger events.
- Chip sleep mode and memory retention mode. AONPD is turned on to retain the contents of a certain memory bank. For example, one of the modes is a reserved mode with a 4kB memory bank. This mode is where the radio works in a sleep state for simple task operations such as advertising or where there is only one connection and the radio works in a sleep state in the most power-efficient manner.
- Chip active mode. All power domains are on.
- Chip off mode. All chip blocks are in a state of power off. The leakage current in this mode is less than 20nA.

3.2.2. Power sequence

The power sequence should follow the sequence as shown in *Figure* 5.

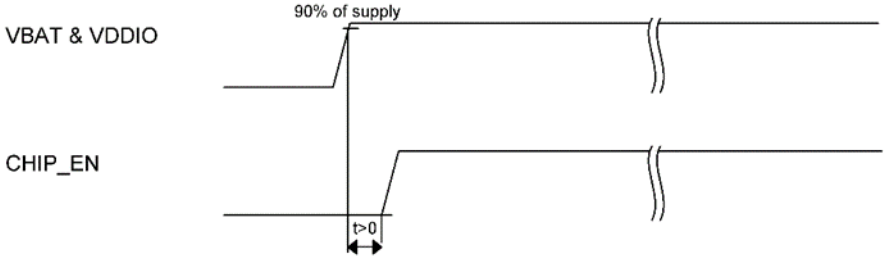


Figure 5 ： Power supply sequence

3.2.3. Power supplies

Figure 6 shows the power architecture for different power domains and blocks. The device has multiple power supplies including VBAT, VDDIO and VDDQ. inside the device, it has a step-down DCDC converter, an AONPD LDO, a retained LDO and two VDDIO switches.

- The AONPD logic is powered by the AONPD LDO.
- The DCDC powers the RF transceiver and the digital core (including the CPU, the digital part of the transceiver, the eFuse, the peripherals) through a digital LDO.
- The memory bank is powered by the digital core LDO in active operation mode and by the retention LDO in sleep mode.
- The two VDDIO switches (VDDIO SW1 and SW2) provide power to the stacked flash memory and external circuits such as sensors. In sleep mode, these two switches can be configured to be turned off to reduce leakage.
- VDDQ is used to program the eFuse memory. It is only needed for eFuse programming. When do the eFuse programming, VDDQ and VDDIO must be 3.3V± 10%.

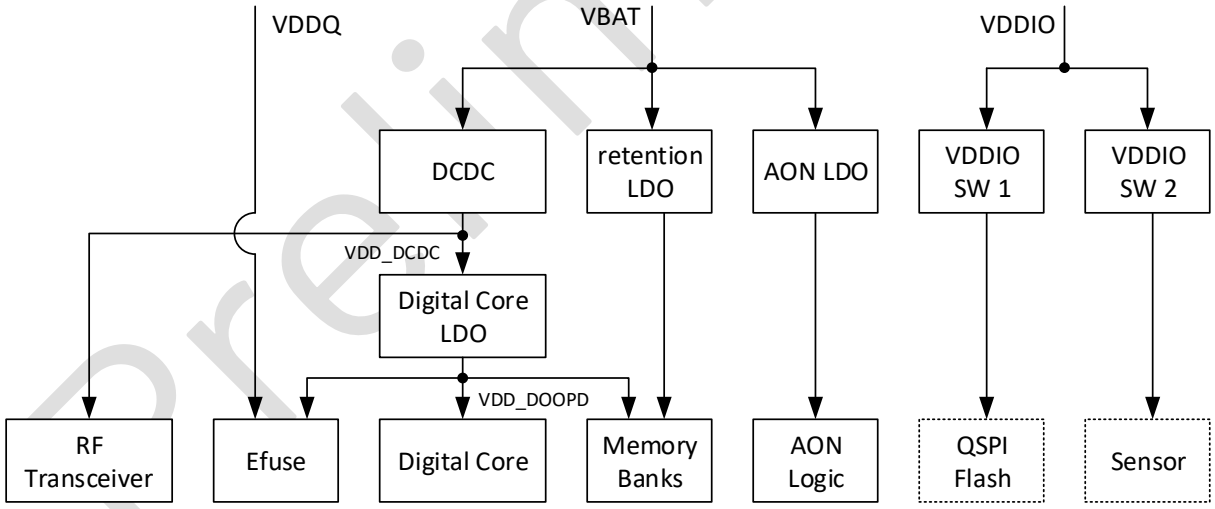


Figure 6 : Device power supplies

3.2.4. DCDC converter

The buck DCDC converter, as shown in *Figure 7*, efficiently reduces the voltage of the battery to around 1.2V. The 1.2V supply is used to power the radio transceiver directly. In addition, it is used as the input to a LDO that in turn creates the supply for the digital core. Two external components are required for the DCDC converter, an inductor and a capacitor. The recommended values are

10uH and 1uF, respectively. Other values are permitted; however, they will affect the behavior of the DCDC in terms of efficiency, startup time, and ripple amplitude.

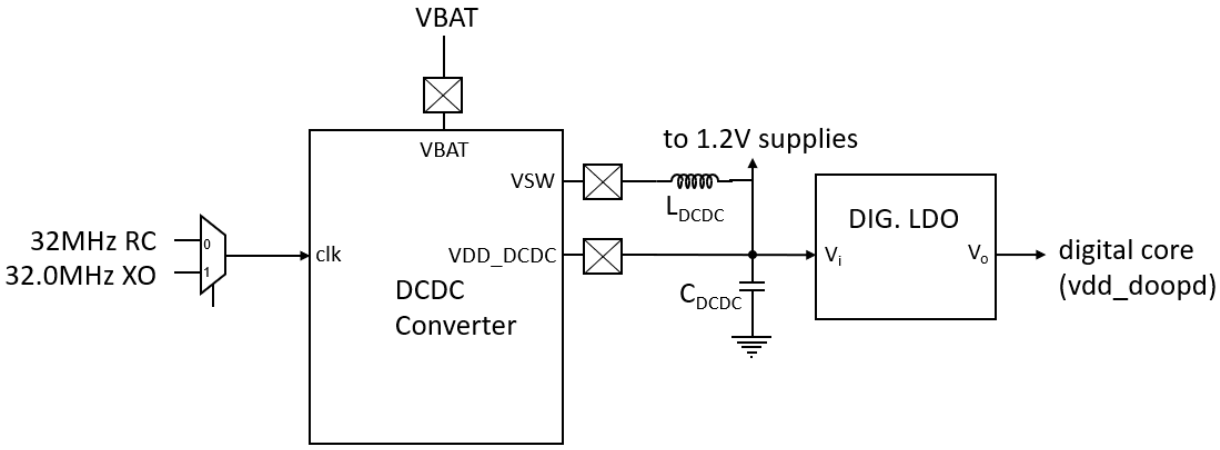


Figure 7：DCDC buck converter

3.2.5. Clock system

The device's clock system is designed to provide clocks to all subsystems that require clocks and for switching between different clock sources without degrading system performance or power consumption.

There are five types of clock sources. They are RC 32kHz, RTC 32.768kHz, RC 32MHz, XO32/64MHz, and Programmable CLK from the clock PLL. RC 32kHz is the default clock for the AONPD.

3.2.5.1. RC 32kHz

The RC32kHz clock is a low frequency clock for AONPD logic. This clock is the default clock source for the AONPD during cold boot. If the eFuse memory configuration indicates that an RTC crystal is installed, the boot code will switch the AONPD clock source to an RTC clock

3.2.5.2. RTC 32.768kHz

At cold boot, RC 32KHz is the default clock for AONPD. After cold boot, the bootrom code will enable the RTC clock if an RTC crystal is installed, and switch to RTC 32.768kHz as the default clock for AONPD. *Figure 8* shows a block diagram of 32.768kHz crystal.

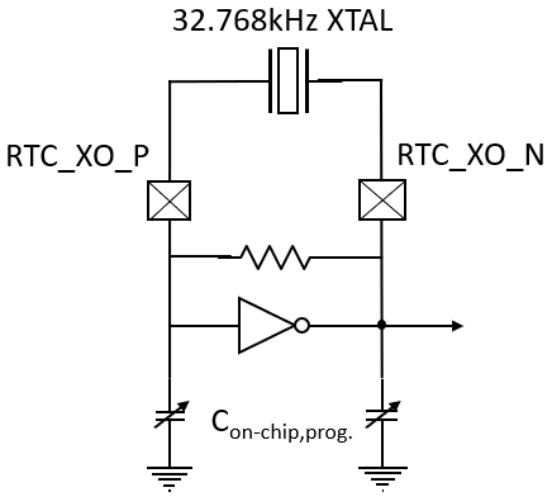


Figure 8 : 32.768kHz crystal

The device also supports external 32.768kHz clock source as input as shown in *Figure 9.*

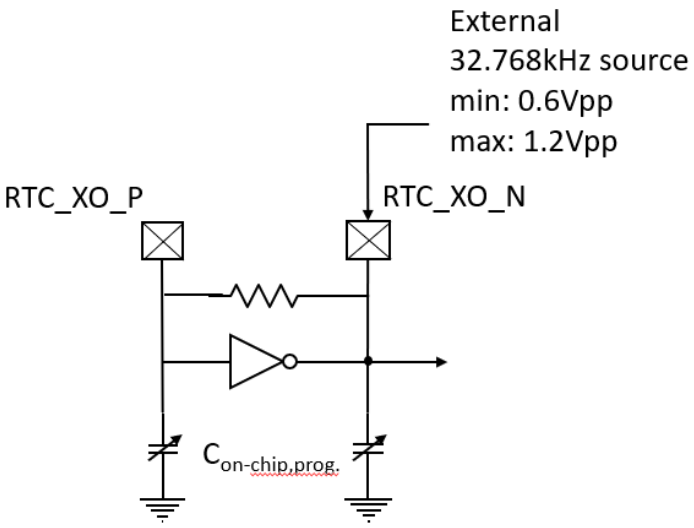


Figure 9 : External 32.768kHz source

The RTC clock can be muxed out to a GPIO pin that user can use for their applications.

3.2.5.3. RC 32MHz

The RC32MHz is a 32MHz high-frequency ring oscillator that provides a clock source during crystal startup. The CPU clock defaults to RC32MHz after cold boot or waking up from sleep mode and can be switched to XO clock after XO stabilization.

3.2.5.4. XO clock

XO clock is high frequency clock source in 32MHz. XO clock is sourced from an external 32MHz crystal as shown in *Figure 10*. XO is controlled by AONPD and is enabled by default after cold boot. The bootloader should switch between the CPU clock and peripheral clock from RC 32MHz to XO 32MHz. This is important for the bootloader as the bootloader may try to get an image from UART interface which requires a more accurate clock source. Inside the chip, we also have one XO doubler which produces the XO 64MHz clock.

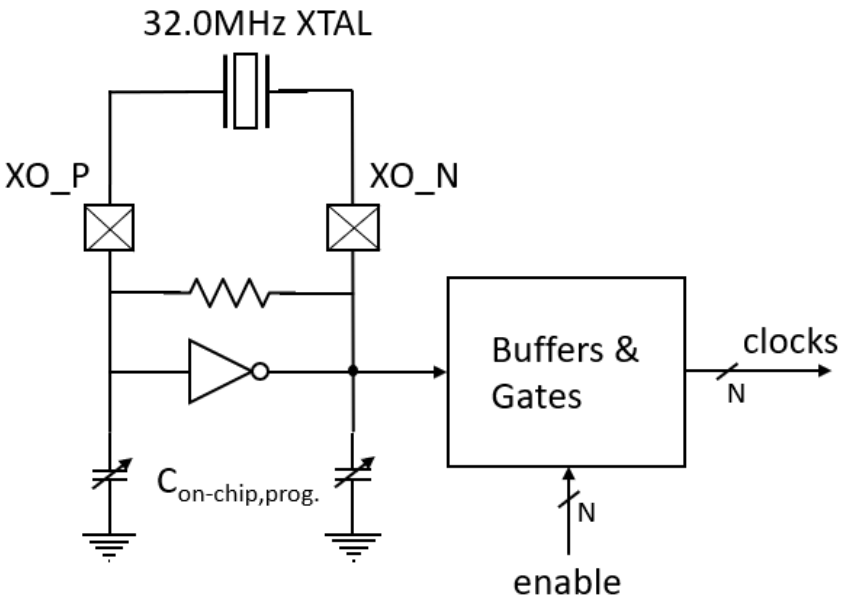


Figure 10：XO clock source

3.2.5.5. CLK PLL

Clock PLL is designed to provide multiple clock frequencies for different clock requirements for the radio transceiver on different PHY rate receptions. By default, CLK PLL is automatically controlled by the hardware.

3.3. Bluetooth 5 radio and subsystem

The device incorporates a Bluetooth Low Energy subsystem that contains the baseband, PHY and link layer engines with an embedded security engine and is fully compliant with Bluetooth Core 5 specification including all the optional features supported such as extended advertising packet length, higher throughput, WLAN coexistence and long-range* mode.

The physical layer has the digital PHY and RF transceiver that transmits and receives GFSK packets at up to 2Mpbs over a 2.4GHz ISM frequency band. The PHY can also be configured to Long-range* mode to transmits and receives either 500Kbps or 125Kbps modulated packets.
The baseband controller combines both hardware and software implementation that supports all device classes (Broadcaster, Central, Observer and Peripheral). And all the timing critical functions are implemented in hardware such as encryption/decryption, FEC decoder, CRC, data whitening and access address detection.

Key BLE5.0 features being supported are as followings:

- Bluetooth Low energy v5.0 specification compliant
- All packet types support (Broadcasting/advertising/data/control/long Range*)
- Advertising packet extension, up to 255 bytes
- Encryption/Decryption (AES-CCM) for enhanced security at link layer
- Bit Stream processing (CRC, whitening)
- WLAN coexistence mechanism (signaling)
- All device roles support (broadcaster, central, observer, peripherals)
- Bluetooth Low Energy v4.0/4.1/4.2 features are fully supported.

The 2.4GHz transceiver has one chip pin, RF_TRX_2G4, for both the transmission and reception of RF signals, as shown in *Figure 11*. An on-board matching network is recommended to get the best RF performance out of the device. It is possible for the matching network to favor the RX path over the TX path or vice-versa, but the recommended matching network in the reference design is a balance of both paths. There are four supply pins for the 2.4GHz transceiver, that are nominally 1.2V. They should normally be connected to the DCDC output, VDD_DCDC. The transceiver needs a 32.0MHz crystal oscillator reference. To reduce BOM cost, the CI for the crystal is integrated on-chip. The on-chip CI can be programmed with registers from 0.5pF to 8pF in 0.5pF steps.

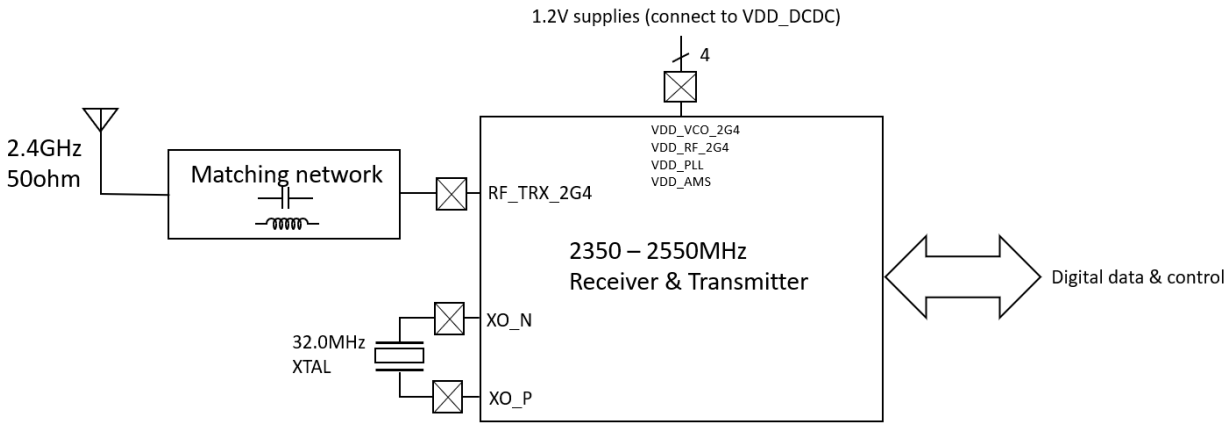


Figure 11 : 2.4GHz RF transceiver

3.4. Software defined radio

The device incorporates a Software Defined Radio (SDR) with which user can have the ability to develop a wireless communication network with their proprietary protocols. The SDR supports GFSK modulation with up to +4dBm as TX power output (2.4Ghz). Also, multiple data rate can be selected such as 125Kbps, 500Kbps, 1Mbps and 2Mbps.

- Event-driven and event-based communication:
  - The data communications among the devices have one or multiple events, as shown in *Figure 12*. Two roles are defined for the InPlay's SDR devices: Initiator and Responder. The device who first starts transmission in an event is called an initiator. The device who always starts from reception is called a responder. The roles of a device can be freely configured by software for different events as shown in *Figure 12*.
  - The initiator can be very low power. Most of the time, it can be in sleep or idle states. Only when there is a need, software can program it to start an event.
- Bluetooth 5 and SDR coexistence
  - The device support BLE and SDR coexistence
- Connectionless communication
  - There is a no need for two devices be connected prior to data communication.
- Multiple TX and RX during an event enables high throughput communication

- During an event, multiple transmissions and receptions are supported as shown in *Figure 12*, which allows multiple packets exchanged between the initiator and the responder.

- Multiple hardware interrupts to facilitate software real-time processing
  - SW programs a device to start an event for data communication. During an event, RX and TX interrupts will be generated once a packet is transmitted or received. At the end, an end of event interrupt will be generated. These interrupts can be used by software for real-time processing.

- Easy software handling
  - Software can start an event any time as long as there is no over-lap. Once an event is started, the hardware state machine takes over the transmission/reception process. If there is no more data packet to be exchanged or there is a time out, the hardware will automatically terminate the event.
  - An event can be also terminated or cancelled by software by just setting a register bit.

- Broadcasting is supported
  - A device can send out broadcasting packets to all other devices

- Private communication with source address and destination address
  - In a network, each InPlay SDR device can be assigned to have a 16-bit address which allows private communication between two devices.

- Low latency and fast response
  - For each event, a responder can prepare and program multiple sets of TX packets. Each set has multiple TX packets, and each set is targeted to a specific initiator. Once a responder receives a packet from an initiator, it will perform an address match automatically and pick the corresponding set of TX packets to communicate to the initiator. This feature enables low-latency and fast response communications. If there is no address match, the responder will simply respond with a packet without payload.
  - During an event, if a responder receives a packet whose destination address does not match the responder address, the responder will simply ignore that packet and continue be in reception mode.

- BLE and SDR coexistence

- The device support BLE and SDR coexistence by flexing hardware and software tools.

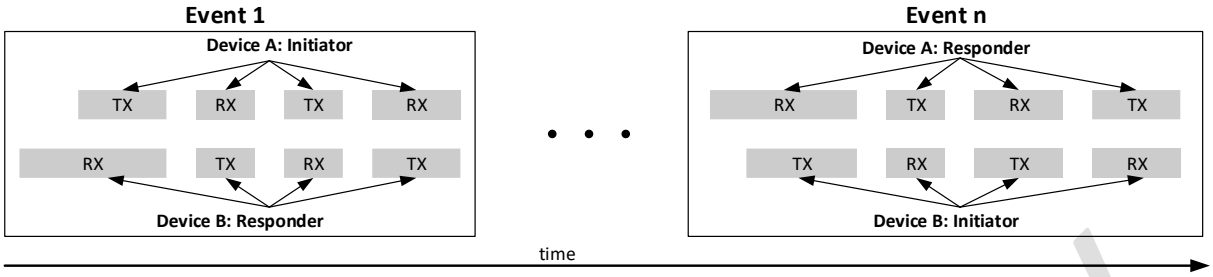


Figure 12 : SDR event and roles

3.5. Arbitrary format TRX

The device supports a flexible transmission and reception which we call arbitrary transmission. The corresponding baseband is called arbitrary transmission BB (ATBB) where the software (SW) can control the packet format of being transmitted. *Figure 13* shows the packet format of the ARBB. The content of sync pattern (also called access address) is defined by the SW. In addition, the SW fully control the content and length of the header, payload and CRC.

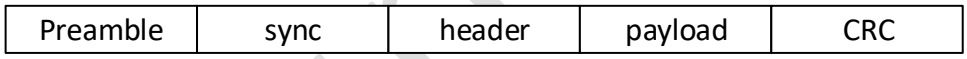


Figure 13 : Packet format for arbitrary TRX

At the receiver side, the SW just needs to specify the expected sync pattern. Once it receives a packet with the expected SYNC pattern, the receiver will sign/al to the CPU.

The channel and PHY rate are also fully programmable and controlled by the SW. Two PHY rates (1Mbps and 2Mbps) are supported.

The arbitrary TRX format enables users to fully control the RF transceiver and develop their own protocol stack.

3.6. Special function blocks

3.6.1. 11-bit sensor ADC

The device has a sensor ADC block as shown in *Figure 14* which user can use for converting analog signals to digital domain signal for CPU processing.

The sensor ADC has 11 physical bits and can convert at a maximum of 64 KSPS. The actual clock speed and conversion rate are controlled through digital settings. The input to the ADC is preceded by a multiplexer which enables the user to sample up to 11 different channels (package option dependent). In addition, the ADC can be used to measure the internal VBAT voltage level or the temperature. The digital control system for the ADC gives the user the flexibility to choose which channels are sampled in what order. The required voltage reference (Vref) to the ADC can be selected from multiple sources, including an on-chip 1.0V reference, the VBAT voltage divided by 2, or external channels. The input voltage range to the ADC shall be between 0V and 2*Vref.

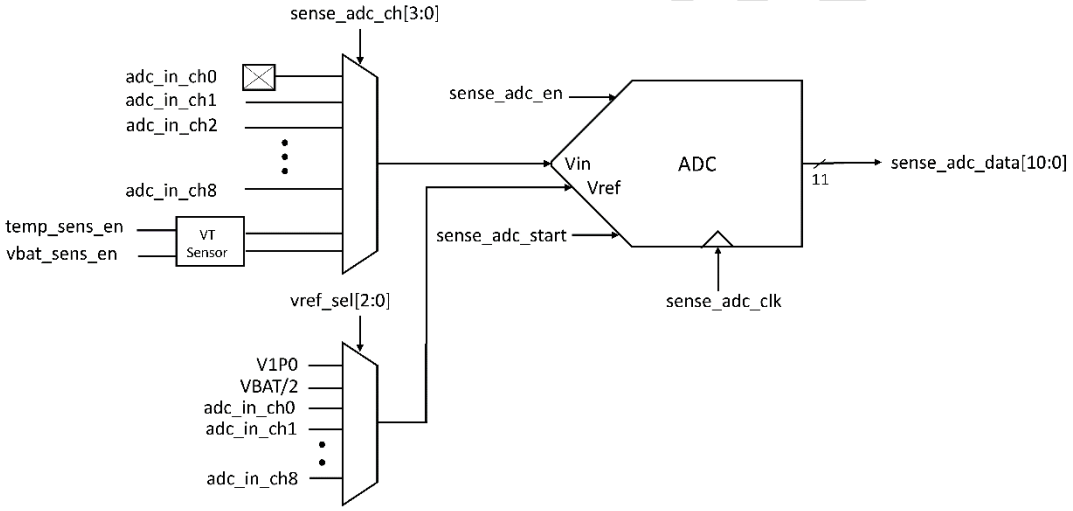


Figure 14 ：Sensor ADC

3.6.2. Hardware security engine

The device integrates a set of cryptographic engines which comprise of hardware accelerator to compute AES, SHA and ECC algorithms. Such engine can be used by user for application that requires strong security system implementation.

The AES module implements AES encryption and decryption algorithm as defined by the NIST FIPS Publication 197. The features supported by this block are.

- Key length supported are 128b, 192b and 256b and is configurable.

- The authentication modes being supported are XCBC, F8, CMAC, CCM, CBC, CTR and ECB mode.

The SHA module implements hash algorithm and supports SHA-1 and SHA-2.

The ECC module implements ECC encryption and decryption algorithm. The key length supported are 128b, 192b and 256 bits.

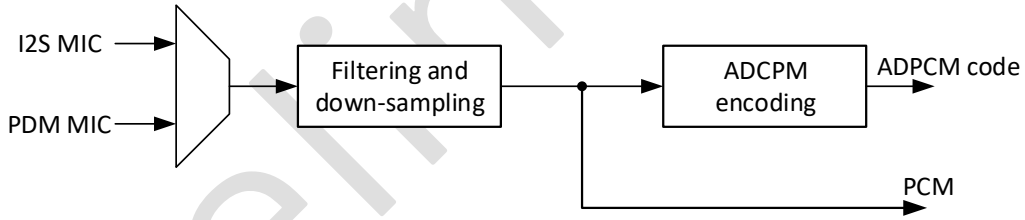
3.6.3. Audio ADPCM and resampling engines

The device has ADPCM and audio sampling rate conversion (SRC) engines which can be used to support and develop wireless voice and audio applications.

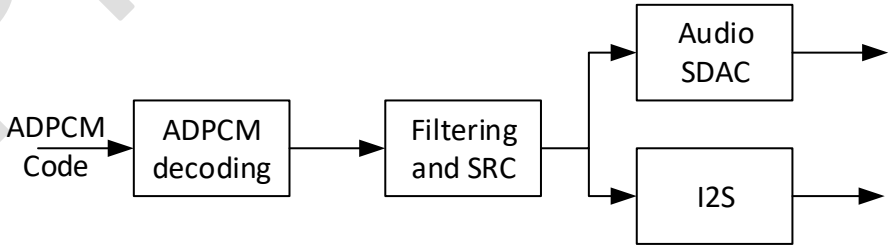
The audio engine takes the audio data input from either PDM or I2S interfaced microphone then do the ADPCM encoding and wrapper for transmission through radio interface as shown in *Figure* 15(a). The ADPCM engine can be bypassed, in that case, we can have raw 16-bit PCM sample outputs.

The received ADPCM coded data through radio interface can also be passed to the ADPCM decoding, and the be played through the Sigma-Delta DAC (SDAC) or I2S as shown in *Figure* 15 (b).

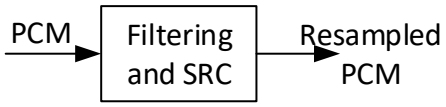
The device's audio SRC can be also to be used for direct PCM sample rate conversion (such as conversion for audio between sampling rate 44.1kHz and 48kHz) as shown in *Figure* 15(c).



(a) ADPCM encoding and PCM output



(b) ADPCM decoding



(c) Audio SRC

Figure 15 : Audio engines

3.6.4. Keyboard controller

The device has a keyboard controller module that scan through the columns or rows to identify each key's row/column index.

User can define the scan interval and scan through all columns/rows every 0.5, 1, 2 or 4 milliseconds. Every time after the scan, if any key status has been updated, an interrupt will be generated to notify the CPU. At the same time, following information will be stored in the status registers:

Table 4 : Key information register format

1 bit (press/release)	1 bit (multi-key event)	28 bits (X/Y index) of the key

The first bit indicates if the key is pressed or released during the scan. The second bit indicates if the multi-key event happens (used to support multiple key pressed/released at the same time). If this bit is asserted, the second status register (same format as the first one) will be populated. If this bit in the second register is also set, the third register will be populated, and so on. At most 4 key status registers will be stored. The last field in the registers is used for column/row index of the key. The number of GPIO's used for columns and rows can be configured through control registers. The number of regular keys and special keys (such as shift, control, alt, home, end, etc.) can be configured through control register and maximal number of supported keys is 108.

Based on the control registers setting, the de-bounce filter can filter out glitches in the range of 0 (de-bounce feature disabled) to 63 milliseconds (in the step of 1ms). The press and release de-bounce filer can have different glitch filtering time value.

All keyboard interrupts will be listed as parallel I/O ports as a standard interrupt controller (including pulse-to-level conversion, masks, clears features) will be used to combine these interrupts to a single interrupt to CPU. All keyboard control and status registers will be used to convert these signals to control/status registers accessible through APB interface to CPU.

3.6.5. Quadrature decoder

The device has a Quadrature Decoder with which user can interface the device to a mechanical to electronical rotary device such as servo motor, volume control wheels and PC mice etc. The

decoded quadrature signals are used as data input to system to determine the absolute or relative position of the rotary device.

The quadrature decoder comprises of Signal_A, Signal_B and Signal_LED as interface pins to external rotary device. Signal_A and Signal_B are input signals from external quadrature encoder to indicate movement of the rotary device. Signal_LED is an optional output signal to external quadrature encoder and will be asserted a few microseconds (defined through control registers) before the sampling and de-asserted immediately after Signal_A, Signal_B values are being sampled by the decoder.

An optional de-bounce filter can be enabled. The Signal_A and Signal_B values are only valid if their values are constants during the de-bounce filter window (which is the same length as the sampling interval). If there is value change in the de-bounce filter window, the Signal_A/Signal_B value will be ignored and keep the same values as the previous sampling. When the de-bounce filter and Signal_LED are enabled, the Signal_LED will keep asserted during the de-bounce filter window and the Signal_A and Signal_B values are kept being sampled.

3.7. Peripherals

3.7.1. I2C

I2C is a simple two-wire bus with a software defined protocol for system control and peripherals. It has a serial data (SDA) and a serial clock (SCL). The device has two independent I2C interfaces (package dependent). The maximum I2C clock rate being supported is 1MHz.

I2C can be configured to operate in either master or slave mode. User has the flexibility to determine and program the slave I2C address. It has 7bit addressing. The slave address is transferred in the first byte after the Start condition. The first seven bits of the byte comprise the slave address with the eighth bit indicating R/W flag ("1" for read and "0" for write). It supports bulk transmit mode.

The I2C has access to the DMA Controller and the data can be moved between CPU memory and peripheral buffer through DMA.

3.7.2. SPI

SPI is a four-wire serial peripheral interface bus commonly used to send data between microcontroller and peripherals. It comprises a clock (SCK) and data lines (MOSI, MISO) along with a chip select line (SS).

The device has two SPI interfaces. They both can be configured to operate on either master mode or slave mode. In master operation mode, the maximum clock rate supported is 16MHz. In the

master mode, the device can support up to 4 independent slaves using different SS line while sharing the same SCK, MOSI and MISO lines. It may also support dual-SPI and quad-SPI mode operation in the master mode to increase the throughput.

In the slave mode, the device can operate on SCK clock rate of no higher than 4MHz.

SPI has access to DMA Controller and the data can be moved between CPU memory and SPI peripheral buffer through DMA.

3.7.3. UART

The device includes two UART cores which supports universal asynchronous transmitter/receiver function and support programmable baud rate up to 2Mbps. The two UART cores are time-multiplexed to 4 UART interfaces (package dependent).

The UART has built-in 16bytes of transmit and receive data FIFO and support auto flow control. The UART has access to the DMA Controller and the data can be moved between CPU memory and UART buffer FIFO buffer through DMA.

3.7.4. Counter/timer/PWM

The device has one 32bit counter which run on the 32MHz XO clock (or divided version of the 32MHz), one 32kHz 32bit counter, and 4 flexibly configurable counters.

The 4 flexibly configurable counters can be used to capture values (and the time duration) of the external slow signals. They can also be used to send signals out based on the configuration registers. They can be used for Infrared remote control (including learning and transmitting) and ISO-7816 protocol. They can also be used for other features such as frequency estimate of external signals, clock generation, delay timing, etc. They can also be chained together to create more complicated signals.

The device has two Sleep Mode Timers. Both can be used by user for implementing Timer functionality in a lower power fashion without waking up the CPU until Sleep Timer Event expires. The clock source for the Sleep Mode Timer can be either from internal RC 32kHz clock or external RTC 32.768kHz clock.

The device has five Pulse Width Modulators (PWMs) with programmable output frequency and duty cycle. The clock source can be from 2MHz up to 32MHz which will provide high resolution of output frequency.

3.7.5. PDM

The device has a PDM interface which can convey audio data digitally over a CLK (clock)/PDM (PDM bit stream) pair. The device supports both mono stream and stereo stream of input from an

external PDM peripheral with multiple PDM clock rate support from 160kHz to 5.12MHz. The PDM bit stream is clocked at a single edge (selectable) for mono stream or clocked at both edges for stereo stream. After filtering and down-sampling, 16-bit PCM stream will be generated which can be further converted to 4-bit ADPCM format.

3.7.6. I2S

The I2S bus is a simple three-wire serial bus protocol used for connecting digital audio devices together. It has SCK (bit clock), WS (Word Select) and SD (serial multiplexed data line). It supports to operate on either master or slave mode. In master I2S mode, the WS clock rate supported are 7.8125kHz, 8kHz, 15.625kHz, 31.25kHz and 46.875kHz. WS clock rate by default is 15.625kHz. The SCK clock supports from a few hundred kHz to 3.2MHz.

The device has two I2S interface. One is master I2S and the other is slave I2S. Both I2S cores support bi-directional data transfer.

The I2S has access to DMA Controller and the data can be moved between CPU memory and I2S data memory through DMA.

3.7.7. Cache and execution-in-place (XIP)

The chip provides a 2-way set associative instruction cache capability for stacked SPI flash to reduce the potential latency due to slower speed on the SPI interface. The cache can support up to 2M bytes of the SPI flash address spaces. The cache data/tag memories can be retained during sleep to speed up wake up CPU execution.

3.7.8. DMA

The chip provides 2 independent DMA controllers and each controller connects to 12 different peripheral interfaces. Each controller also provides 2 parallel channels which can be enabled simultaneously. The DMA controllers supports data copy between peripheral buffers, shared memories and the CPU data memories. All channels in the DMA controllers supports multi-block DMA transfers.

3.7.9. WDT

A programmable WDT is provided, and its timeout signal is connected to Cortex M4 non-maskable interrupt (NMI) source. The second timeout signal from WDT can also be programmed to be sent through chip pins (polarity programmable) for external hardware logic to reset the chip. It can also be sent out as a periodic waveform as preprogramed in PWM block. The same signal can also be programmed to reset the whole chip automatically or switchable power domain.

3.7.10. Audio encoder/decoder

Simple adaptive differential pulse-coded modulation (ADPCM) audio encoder/decoder is provided as low-quality audio digital MIC/speaker interface. Multiple commercial ADPCM packet formats

including Microsoft and Apple are supported. Raw PCM format data from digital MIC interface (through PDM or I2S) is also provided and available to CPU processing through DMA or manually memory read.

3.7.11. GPIO and analog I/O

The device supports up to 30 GPIOs (package dependent) and a dedicated analog input pin (package dependent). There are two types of GPIOs: mixed signal GPIOs and digital general purpose IOs. A mixed signal GPIO can be configured as a digital GPIO or be configured as an analog signal input pin for Senor ADC.

Each GPIO has a programable pullup or pulldown resistor when it is in digital input mode and has a 2-level programmable output driving strength options.

Each GPIO can be configured as a wakeup pin, and the polarity of each wakeup signal can be programmable to “high” or “low”.

The device supports GPIO state retention during sleep.

All GPIOs support asynchronous interrupts. They can be configured as interrupt sources to the ARM core. Multiple of GPIOs’ inputs can be grouped together to form a single interrupt. For each GPIO’s input, we can configure its polarity, and its mask.

When CHIP_EN (chip enable) is low, the device is in shutdown mode and all the GPIO(s) are in high Z output state. When the chip is enabled, all the GPIOs are in input mode by default (with pull-up enabled). After boot, the SW may program the GPIOs as appropriate modes (like input/output/high Z state or analog input).

3.8. Programing and debugging interface

Debug and trace functions are integrated into the device. Serial Wire Debug (SWD) and JTAG (Trace functions) are supported.

Note that SWD and JTAG will be disabled once an eFuse bit (the JLINK disable bit) is programmed to be 1, and there will be no access allowed by and from external debugging tools.

3.9. User software copyright protection and secure boot

Often, for a system with a flash memory, there are two concerns. The first concern is to how to protect the IPs on the flash memory. To protect IPs on the flash memory, one of popular approaches is to encrypt the code. The second concern is that we need to make sure the image on the flash is an authenticate image. To resolve the second concern, secure booting is required.

The device supports flash encryption and secure booting which can be used to protect user's IP and authenticate the image before it is executed.

3.9.1. User software copyright protection

The device has a dedicated encryption engine that protects the user's software intellectual property. It supports secure file transfer from programmer to device, as shown in *Figure 16*. When a programmer attempts to program the device's flash memory, the program and the device's bootrom can negotiate a shared key through the ECDH (Elliptic-Curve Diffie-Hellman) key exchange protocol. The key can then be used to encrypt the firmware image file as the programmer transfers it to the device. The encryption is based on AES-256.

The IN6XX series devices have a dedicated random number generator. Each time the key is negotiated with the programmer, it will use a different random number. As a result, the different device will have different keys at different times.

Figure 16 : Secure software copyright protection

The firmware image file stored on the stacked flash memory can be configured to be encrypted or unencrypted fashion. If choose to be encrypted, when the device's bootrom gets an encrypted image from the programmer, it first decrypts the image file, and then re-encrypts the image using different key generated through secure programming key generator engine. The newly encrypted image will be programmed to the stacked flash menory. Such procedure is being defined as secure programing.

Two types of flash encryption are supported: One is AES-256 encryption. When executing the AES-256 encrypted code, the bootrom will first decrypt the encrypted code using a secret key tied with device's unique ID and put the decrypted code on the device's internal RAM. Another type of encryption is InPlay's Proprietary Real-Time Encryption (PRTE) which can be decrypted on real-time code execution. An image can be configured to be partly AES-256 encrypted, partly InPlay's PRTE encrypted, or partly non-encrypted. The encryption keys are tied with the device's unique ID. Thus, the same encrypted code will not be executed on two different devices. We call such code execution on the device secure execution.

3.9.2. Secure boot

The device supports secure boot based on user's choice. To support secure boot, a firmware image needs to be signed by an encrypted signature (called certificate) attached with that firmware image, as shown in *Figure* 17. During cold boot, the bootrom authenticate the signature.

If the authentication fails, the bootrom stops the booting process. The device has dedicated hardware engine and bootrom code to support secure boot.

As shown in Figure 17, to support secure boot, a signature must be generated using certain hash engine such as SHA-2. The signature is then encrypted by using ECC (elliptic curve cryptography) encryption. The encrypted signature is a certificate. That certificate will be attached to the image and be programmed into the device's stacked flash memory. The signature is encrypted by using a private key. The corresponding public key shall be programmed into the device's internal eFuse memory, and the eFuse can be configured to lock the public key so that it cannot be modified or altered.

During cold boot, the bootrom hashes the image on the flash memory to calculate its signature. Then, the bootrom uses the ECDSA (Elliptic Curve Digital Algorithm) to authenticate and verify the signature based on the certificate, and the public key. If the verification process passes through, the bootrom will boot the image.

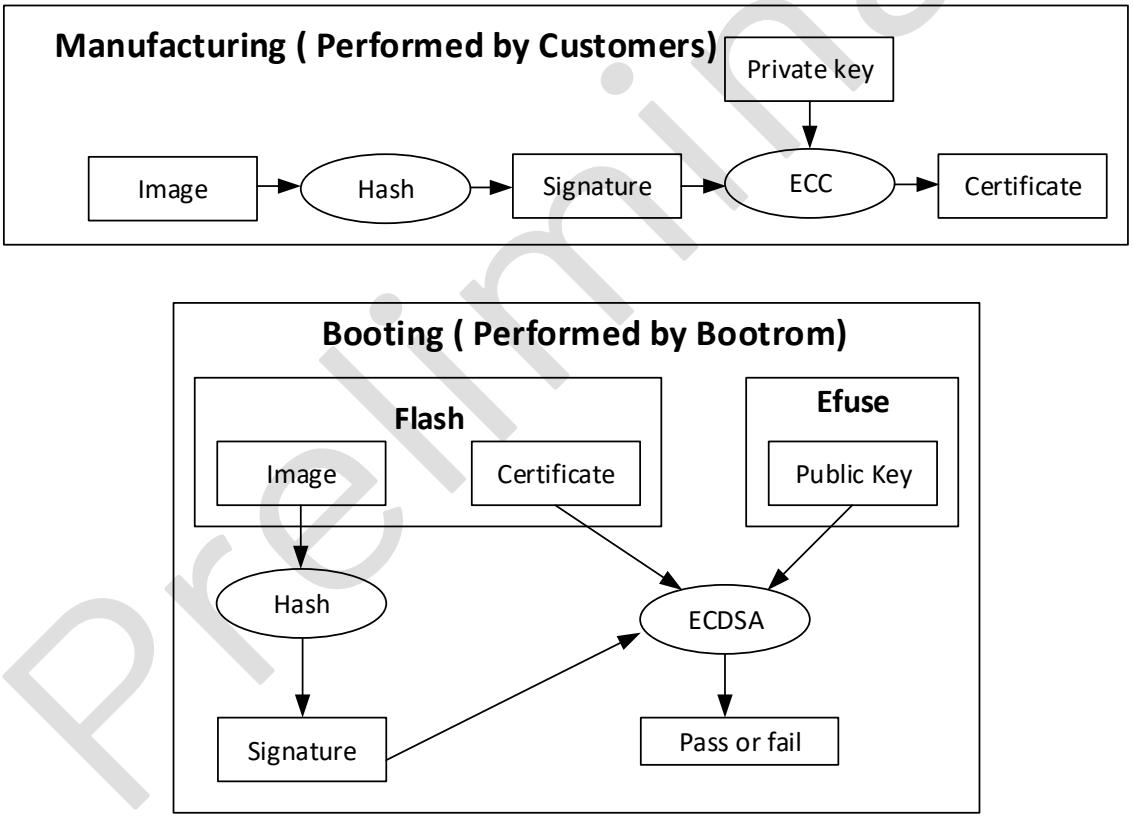


Figure 17 : Secure boot

4. Electronical Characteristics

There are voltage ranges where different VDDIO levels apply. The reason for this separation is for the IO drivers whose drive strength is directly proportional to the IO supply voltage. In the IN602 products, there is a large gap in the IO supply voltage range (1.7 to 3.6v). A guarantee on drive strength across this voltage range would be intolerable to most vendors who only use a subsection of the IO supply range. As such, these voltages are segmented into three manageable sections referenced as VDDIOL, VDDIOM, and VDDIOH in tables listed in this document.

4.1. Absolute maximum ratings

The values listed in this section are the ratings at which the chip can peak, and stresses listed above the absolute maximum rating may cause permanent damage to the device. Functional operation of the device should follow the conditions indicated in the "Recommended Operating Conditions", prolonged exposure to the absolute maximum rating may affect the reliability of the device.

Table 5 : Absolute maximum ratings

Description	Comments	Min.	Max.	Unit
Supply voltage (VDDIO1, VDDIO2)		-0.3	3.9	V
Supply voltage (VBAT)		-0.3	3.9	V
Digital GPIO input	All digital GPIO pins	-0.3	VDDIO+0.3	V
Analog HV input	CHIP_EN	-0.3	VBAT	V
TRX Supply voltage	VDD_RF_2G4, VDD_VCO_2G4, VDD_PLL, VDD_AMS	-0.3	2	V
Analog LV input	XO_N, XO_P, RTC_XO_N, RTC_XO_P, , ADC_IN *MGPIO_2_X	-0.3	2	V
Input RF level	RF_TRX_2G4		5	dBm
ESD Human Body Model	All pins	-4000	4000	V
Storage Temperature		-65	150	°C

Note:* The MGPIO_2_X Used as ADC_IN, The input Voltage should less than 2V

4.2. Recommended operating conditions

Table 6 : Recommended operating conditions

Description	Min.	Typ.	Max.	Unit
I/O supply voltage	1.7	3	3.6	V
Battery supply voltage	1.7	3	3.6	V
Operating temperature	-40		85	℃

4.3. GPIO PAD characteristics

Measured at the following condition: Ta = 25°C, VBAT = 3.0V, L=4.7uH, C=4.7uF, unless otherwise noted.

Table 7 : GPIO PAD characteristics

Parameter	Description	Min.	Typ.	Max.	Unit
VIL	Input low voltage			0.3*VDDIO	V
VIH	Input High voltage	0.7*VDDIO			V
VOL	Output low voltage			0.4	V
VOH	output high voltage	VDDIO-0.4V			V
IOH	Output high drive current		4		mA
IOS	Output standard drive current		4		mA
tLH/tHL (standard drive)	Rising time/Falling time @standard drive with 12pf load 10%~90%			4	ns
tLH/tHL (high drive)	Rising time/Falling time @high drive with 12pf load 10%~90%			3	ns
RPU	GPIO Pull-up resistance		21K		Ohm
RPD	GPIO Pull-down resistance		25K		Ohm

Note: The data measured are preliminary and subject to change

4.4. Buck converter characteristics

Measured at the following condition: Ta = 25°C, VBAT=VDDIO=3.0V, L=4.7uH, C=4.7uF, unless otherwise noted.

Table 8 ：Buck converter characteristics

Parameter	Test conditions	Min.	Typ.	Max.	Unit
Output current capability		0	15	30	mA
External capacitor range		1	4.7	20	uF
External inductor range		2	4.7	10	uH
Inductor ESR			300	650	MOhm
Inductor saturation current		150		500	mA
VBAT		1.7	3.0	4.3	V
Output voltage range		1	1.2	1.4	V
Efficiency @3.0V VBAT			83		%
Efficiency @1.8V VBAT			89		%
Startup time			250	400	us
Overshoot at startup			0		V

4.5. 11-bit SAR ADC characteristics

Measured at the following condition: Ta = 25°C, VBAT=VDDIO=3.0V, VREF=on-chip V1P0, unless otherwise noted (If the ADC is used, VBAT should not be larger than 3.0V).

Table 9：ADC characteristics

Parameter	Test conditions	Min.	Typ.	Max.	Unit
Physical bits			11		bits
ENOB	64 KSPS		9.7		bits
	32 KSPS		10.3		bits
SINAD	64 KSPS		60.0		dB
	32 KSPS		63.3		dB
Current from VBAT	64 KSPS		123		uA
	32 KSPS		122		uA
Current from 1.2V VDD	64 KSPS		900		nA
	32 KSPS		460		nA

Parameter	Test conditions	Min.	Typ.	Max.	Unit
Conversion latency		13			clock cycles
Conversion rate			64		KSPS
INL		-2		2	LSB
DNL		-1		1	LSB
VREF	Select by register control: External or internal		1.0	VBAT/2	V
Input voltage range		0		2*VREF	V
Input channels				11 (*1)	-
Input signaling	single-ended		-		
Input offset			10		mV

Note:

(1*): Number of channels depends on package

4.6. VBAT monitoring characteristics

Measured at: Ta = 25°C, VBAT=VDDIO=3.0V, unless otherwise noted.

Table 10 : Vbat monitoring characteristics

Parameter	Test conditions	Min.	Typ.	Max.	Unit
Resolution	Using on-chip V1P0 as reference		2.3		mV/LSB
Range	Input to ADC = 0.4*VBAT. Input range of ADC is 0V - 2V (FS).	1.7		3.6	V
Accuracy	With VREF calibration only	-3.3	1.1	3.3	%
	With ADC offset and VREF calibration	-0.6	0.2	0.6	%

4.7. Device temperature monitoring characteristics

Measured at: Ta = 25°C, VBAT=VDDIO=3.0V, unless otherwise noted.

Table 11 ： Temperature monitoring characteristics

Parameter	Test conditions	Min.	Typ.	Max.	Unit
Resolution	Using on-chip V1P0 as reference		-0.25		°C /LSB
Range		-40		85	°C
Accuracy	With VREF calibration only	-3	1	3	%
	With ADC offset and VREF calibration	-1.8	0.6	1.8	%

4.8. 32kHz RC oscillator characteristics

Measured at the following condition: Ta = 25°C, VBAT=VDDIO=3.0V, unless otherwise noted.

Table 12 ： 32kHz RC oscillator characteristics

Parameter	Test conditions	Min.	Typ.	Max.	Unit
Oscillation frequency	Calibrated with code: osc_32kHz_rc_ibg = TBD, osc_32kHz_rc_ictat = TBD		32		kHz
Temperature coefficient	Calibrated with code: osc_32kHz_rc_ibg = TBD, osc_32kHz_rc_ictat = TBD		TBD		ppm/°C

4.9. 32MHz crystal oscillator characteristics

Measured at the following condition: Ta = 25°C, VBAT=VDDIO=3.0V, unless otherwise noted.

Table 13 ： 32MHz Crystal oscillator characteristics

Parameter	Test conditions	Min.	Typ.	Max.	Unit
Crystal frequency			32		MHz
Crystal frequency tolerance		-40		40	ppm
ESR			60		Ohm

Parameter	Test conditions	Min.	Typ.	Max.	Unit
Lm, motional inductance	(*1)		17	35	mH
Cm, motional capacitance	(*1)		2.2	3	fF
Cl crystal load capacitance	(*1), differential			8	pF
C0	(*1)		0.7	3	pF
On-chip Cl	differential, programmable in 0.5pF steps	0.5		8	pF
Start-up time			500	1000	us

Note: (1*): Crystal datasheet must meet these requirements.

4.10. 32MHz RC oscillator characteristics

Measured at the following condition: Ta = 25°C, VBAT=VDDIO=3.0V, unless otherwise noted.

Table 14 ： 32MHz RC oscillator characteristics

Parameter	Test conditions	Min.	Typ.	Max.	Unit
Oscillation frequency	Programmable with 1MHz resolution	16	32	48	MHz
Temperature coefficient			TBD		%/°C

4.11. 32.768kHz RTC oscillator characteristics

Measured at the following condition: Ta = 25°C, VBAT=VDDIO=3.0V, unless otherwise noted.

Table 15 ： 32.768kHz RTC oscillator characteristics

Parameter	Test conditions	Min.	Typ.	Max.	Unit
Crystal frequency			32.768		kHz
Crystal frequency tolerance	Including aging and temp. drift	-500		500	ppm
ESR			30	100	kOhm

Parameter	Test conditions	Min.	Typ.	Max.	Unit
On-chip CI	differential, programmable in 0.5pF steps	0.5		16	pF
CI crystal load capacitance	differential	4	7	12	pF

4.12.RF performance characteristics

Characteristics are measured over recommended operating conditions unless otherwise specified. Typical value is referred to at TA = 25°C and VBAT = 3.0V. The specifications are valid for -45°C ≤ TA ≤ +85°C and 1.8V ≤ VBAT ≤ 3.6V. All performance data are measured via an evaluation board with a 50 Ohm antenna connector.

4.12.1. General RF characteristics

Table 16 ： General RF characteristics

Parameter	Description	Min.	Typ.	Max.	Unit
Radio frequency range		2320		2650	MHz
RF PLL channel spacing	channel spacing is user programmable		1		MHz
Frequency modulation deviation	1Mbps PHY		±250		kHz
Frequency modulation deviation	2Mbps PHY		±500		kHz
Data Rate		125		2000	kbps
RSSI dynamic range		-100		-25	dB
RSSI accuracy			2		dB
RSSI resolution			1		dB

4.12.2. RF receiver Performance Characteristics

Measured at: Ta = 25°C, VBAT=VDDIO=3.0V, fRF=2440MHz, unless otherwise noted.

Table 17 : RF receiver performance characteristics

Parameter	Condition	Test conditions	Min.	Typ.	Max.	Unit
Maximum receive signal level	1Mbps			5		dBm
Sensitivity - typ. current setting	2Mbps	Average of all channels. Using on-chip DCDC. Measured at SMA connector, BER=1e-3. Typical current settings.		-94.5(*1)		dBm
	1Mbps			-97.5(*1)		dBm
	500kbps			-100		dBm
	125kbps			-104		dBm
Sensitivity Improvement delta - max. current setting		Set LNA bias current to maximum		-0.5		dB
Sensitivity build-to-build variation		Chip variation + matching component variation	-0.5		0.5	dB
I/D Co-channel	2Mbps	Desired signal at -67dBm, modulated interferer in channel, BER=1e-3		-7.6		dB
I/D Selectivity, +/- 2MHz				8 / 4		dB
I/D Selectivity, +/- 4MHz				45 / 15		dB
I/D Selectivity, +/- 6MHz				49 / 35		dB
I/D Selectivity, +/- 8MHz				52 / 43		dB
I/D Selectivity, +/- 16MHz				44 / 36		dB
I/D Selectivity, +/- 32MHz				53 / 51		dB
I/D Selectivity, +/- (10..20)MHz				41		dB
I/D Selectivity, +/- (21+)MHz				50		dB

Parameter	Condition	Test conditions	Min.	Typ.	Max.	Unit
I/D Selectivity, image frequency				15		dB
I/D Selectivity, adjacent (2MHz) to image frequency				35		dB
I/D Co-channel	1Mbps	Desired signal at -67dBm, modulated interferer in channel, BER=1e-3		-6.2		dB
I/D Selectivity, +/- 1MHz				5.6 / 3.6		dB
I/D Selectivity, +/- 2MHz				42 / 23		dB
I/D Selectivity, +/- 3MHz				47 / 32		dB
I/D Selectivity, +/- 4MHz				50 / 37		dB
I/D Selectivity, +/- 16MHz				54 / 53		dB
I/D Selectivity, +/- (5..10)MHz				45		dB
I/D Selectivity, +/- (11..20)MHz				55		dB
I/D Selectivity, +/- (21+)MHz				56		dB
I/D Selectivity, image frequency				23		dB
I/D Selectivity, adjacent (1MHz) to image frequency				32		dB
I/D Co-channel	500kbps	Desired signal at -72dBm, modulated interferer in channel, BER=1e-3		-2.5		dB
I/D Selectivity, +/- 1MHz				9 / 7		dB
I/D Selectivity, +/- 2MHz				47 / 32		dB
I/D Selectivity, +/- 3MHz				51 / 39		dB
I/D Selectivity, +/- 4MHz				54 / 43		dB
I/D Selectivity, +/- 16MHz				49 / 44		dB

Parameter	Condition	Test conditions	Min.	Typ.	Max.	Unit
I/D Selectivity, +/- 32MHz				61 / 60		dB
I/D Selectivity, +/- (5..10)MHz				48		dB
I/D Selectivity, +/- (11..20)MHz				52		dB
I/D Selectivity, +/- (21+)MHz				55		dB
I/D Selectivity, image frequency				32		dB
I/D Selectivity, adjacent (1MHz) to image frequency				39		dB
I/D Co-channel	125kbps	Desired signal at -79dBm, modulated interferer in channel, BER=1e-3		-1.5		dB
I/D Selectivity, +/- 1MHz				12.5/ 10.5		dB
I/D Selectivity, +/- 2MHz				51 / 33		dB
I/D Selectivity, +/- 3MHz				54 / 39		dB
I/D Selectivity, +/- 4MHz				57 / 46		dB
I/D Selectivity, +/- 16MHz				49 / 45		dB
I/D Selectivity, +/- 32MHz				63 / 62		dB
I/D Selectivity, +/- (5..10)MHz				52		dB
I/D Selectivity, +/- (11..20)MHz				55		dB
I/D Selectivity, +/- (21+)MHz				68		dB
I/D Selectivity, image frequency				39		dB
I/D Selectivity, adjacent (1MHz) to image frequency				46		dB
Intermodulation	2Mbps	Desired at 2402MHz, -		-32		dBm

Parameter	Condition	Test conditions	Min.	Typ.	Max.	Unit
		64dBm. Two interferers at 2408MHz (N+3) and 2414MHz (N+6) at the given power level				
	1Mbps	Desired at 2402MHz, -64dBm. Two interferers at 2405MHz (N+3) and 2408MHz (N+6) at the given power level		-27		dBm
Out-of-band blocking	1Mbps	30MHz *(1) to 2000MHz, step = 10MHz		-10		dBm
		2003MHz to 2399MHz, step = 3MHz		-5		dBm
		2484MHz to 2997MHz, step = 3MHz		-10		dBm
		3000MHz to 12.75GHz *(2), step = 25MHz		-8		dBm

Note: (1*): LNA max gain setting

4.12.3. RF Transmitter Performance Characteristics

Measured at: Ta = 25°C, VBAT=VDDIO=3.0V, fRF=2440MHz, unless otherwise noted.

Table 18 ： RF transmitter performance characteristics

Parameter	Condition	Test conditions	Min.	Typ.	Max.	Unit
Maximum output power		Averaged over band and build		3		dBm
Minimum output power				-35		dBm
Output power variation over band		2402MHz - 2480MHz	-0.5		0.5	dB

Parameter	Condition	Test conditions	Min.	Typ.	Max.	Unit
Output power build-to-build variation		Chip variation + matching component variation	-0.5		0.5	dB
In-band spurious emission	2Mbps, @ Pout,max	N +/- 4MHz		-44		dBm
		N +/- 5MHz		-46		dBm
		N +/- ≥6MHz		-48		dBm
In-band spurious emission	1Mbps, @ Pout,max	N +/- 2MHz		-38		dBm
		N +/- ≥3MHz		-41		dBm
Out-of-band spurious emission	@ Pout,max	f<1GHz, outside restricted bands		-67		dBm
		f<1GHz, restricted bands ETSI		-77		dBm
		f<1GHz, restricted bands FCC		-63		dBm
		f>1GHz, including harmonics		-44		dBm
		HD2		-48		dBm
		HD3		-45		dBm

4.13. System power consumption

Currents are measured at Ta = 25°C, VBAT = VDDIO = 3.0V, CPU running at 8MHz with internal DC-DC converter enabled, unless otherwise noted.

Table 19 ： System power consumption

Parameter		Test conditions	Min.	Typ.	Max.	Unit
I_VBAT	Current consumption	Chip disabled, CHIP_EN=0V		20		nA
		Sleep with 32kHz RC, sleep timer (*1)		0.52 (*2)		uA
		Sleep with 32.768kHz RTC, sleep timer (*1)		0.64 (*2)		uA

Parameter		Test conditions	Min.	Typ.	Max.	Unit
		Sleep with 32.768kHz RTC, sleep timer, 16kB retention (*1)		0.80 (*2)		uA
		Sleep with 32.768kHz RTC, sleep timer, 32kB retention (*1)		0.94 (*2)		uA
		Sleep with 32.768kHz RTC, sleep timer, 32kB retention, BOD enabled (*1)		1.34 (*2)		uA
		Idle. DCDC powers up core and RAM, 32MHz XO not running		500 (*2)		uA
		Active. 32MHz running and core running CoreMark		X mA + Y uA/MHz		
		2.4GHz RX mode - 1Mbps (*3)		7.0		mA
		2.4GHz RX mode - 1Mbps (*4)		7.3		mA
		2.4GHz RX mode - 2Mbps		8.3		mA
		2.4GHz TX mode - 1Mbps, Pout=0dBm		6.5		mA
		2.4GHz TX mode - 1Mbps, Pout=max		9.5		mA
		2.4GHz TX mode - 2Mbps, Pout=0dBm		6.6		mA
		2.4GHz TX mode - 2Mbps, Pout=max		9.6		mA
I_VDDIO	VDDIO current consumption	Chip disabled, CHIP_EN=0V		10		nA

Note:

(1*): VDD_AONPD is in dynamic mode

(2*): Number is based on C/S measurement

(3*): Settings for -97dBm sensitivity

(4*): Settings for -97.5dBm sensitivity

4.14. ESD characteristics (all pins)

- HBM (human body model): Sensitivity pass +/-4500V, Class-3A (Reference ESDA/JEDEC JS-001-2017)
- CDM (charge device model): Sensitivity Pass: ±1000V, Class-C3 ESDA/JEDEC JS-002-2018

5. Ordering Information

Table 20 Ordering Information contains information on IC marking and ordering codes. *Figure* 18 provides all the available package options for developers to choose from.

Table 20 ： Ordering information

Part number	Bluetooth 5 (Y/N)	Long range*	SDR (Y/N)	Flash memory	Package
IN612L	Yes	Yes	Yes	Yes	See *Table 21*
IN610L	Yes	Yes	No	Yes	See *Table 21*
IN610	Yes	No	No	Yes	See *Table 21*
IN600	Yes	No	No	No	See *Table 21*

* Long-range modes (125Kbps & 500Kbps)

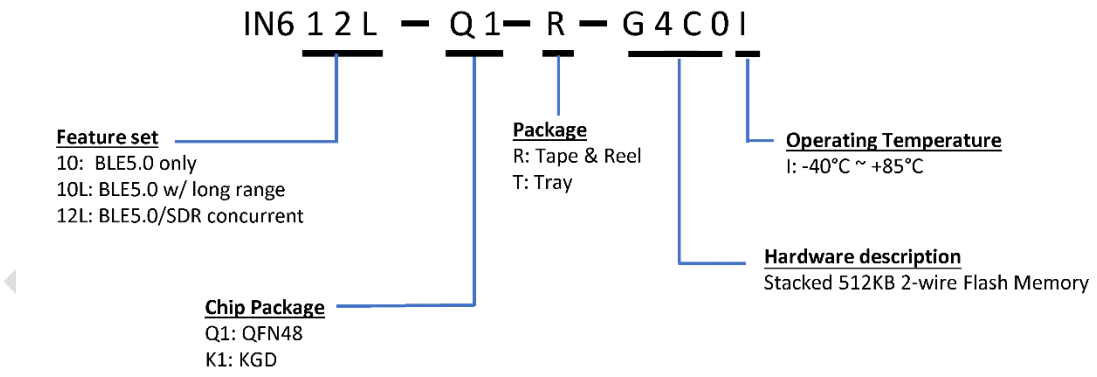


Figure 18 ： Full ordering part number decoder

6. Packaging

The device will be offered in QFN48 packages. The QFN package is RoHS/green compliant.

6.1. Package drawing – QFN48

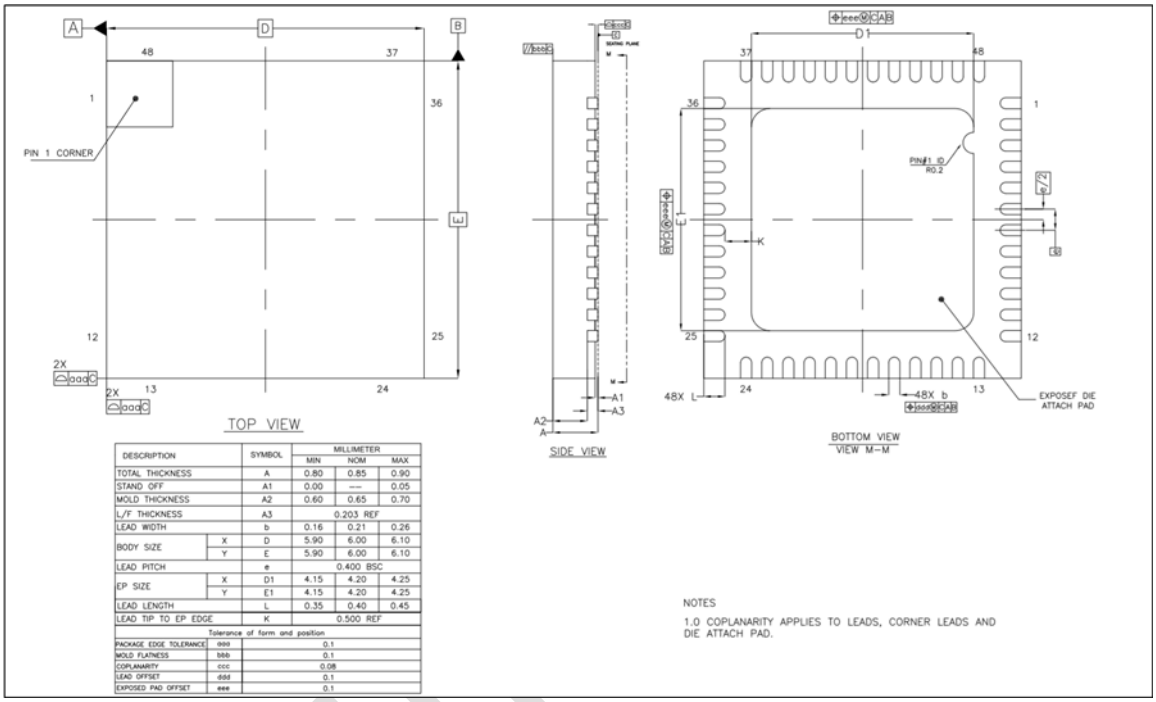


Figure 19 ： IN612L QFN48 6mmx6mm package outline drawing

Table 21 ： IN612L 6x6 QFN48 package information

Parameter	Value	Units	Tolerance
Package Size	6.00 x 6.00	mm	±0.10
QFN Pad Count	49		
Total Thickness	0.85	mm	±0.05
QFN Pad Pitch	0.40	mm	
Lead Width	0.21	mm	±0.05
Exposed Pad Size	4.20 x 4.20	mm	±0.05

6.2. IC marking

The IN612L IC is marked like described below, as shown in in *Figure 20*.

Figure 20 ： IN612L package marking

Table 22 ： IN612L marking description

Abbreviation	Definition and implemented codes
IN6XX-Q1	INPLAY SwiftRadio™ SoC product name
AG	Vender code
YY	Year code
WW	Week code
R	Die version
I	Temperature code
MXXX.XXX	Production control code

6.3. Box package dimension

Defined here are the device package size for reel, inner box and outer box.

Table 23 ： IN612L package size for reel, inner box and outer box

Package	Reel size	Reel size	Inner box size	Outer box size
QFN	13″	4000	4000	40000

7. Reference Design

7.1. IN612L QFN48 reference schematic

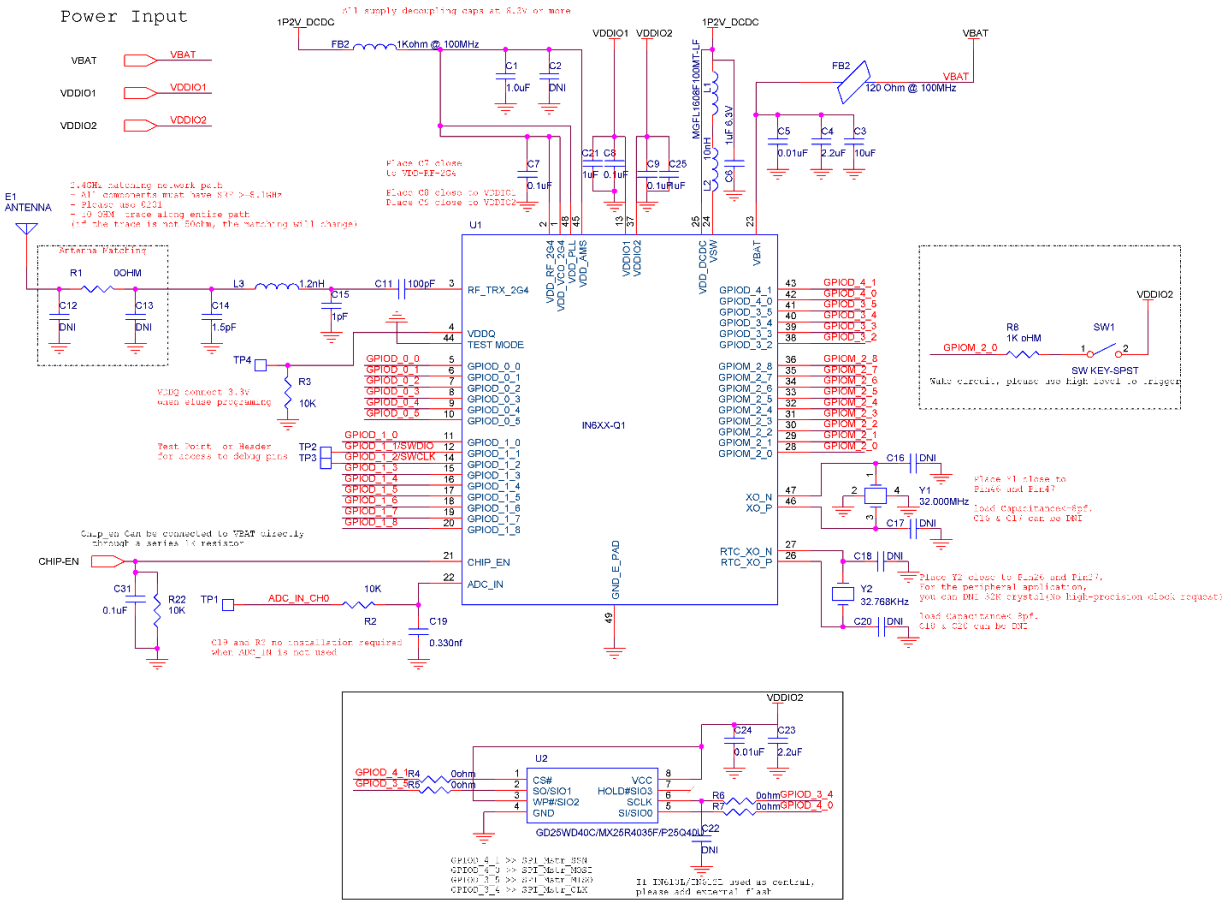


Figure 21：IN612L/IN610L/IN610 QFN48 reference schematic

Table 24：IN612L/IN610L/IN610 reference design BOM of QFN48

Reference	Value	Description	Vendor	Part number	Foot print
C1	1.0uF	Cap cer 1uF 6.3V X5R	Murata	GRM033R60J105MEA2D	C0201
C2,C12,C13,C10,C16,C17,C18,C20	DNI	Do not insert			
C3	10uF	Cap cer 10uF 6.3V JB	TDK	C1608JB0J106M080AB	C0603

Reference	Value	Description	Vendor	Part number	Foot print
C4	2.2uF	Cap cer 2.2uF 6.3V X7S	TDK	C1005X7S0J225K050BC	C0402
C5	0.01uF	Cap cer 10000pF 10V X7R	Murata	GCM033R71A103KA03D	C0201
C6	1uF	Cap cer 1uF 25V X5R 0402	TDK	C1005X5R1E105KT000E	C0402
C7,C8,C9	0.1uF	Cap cer 0.1uF 6.3V X6S	Murata	GRM033C80J104ME15D	C0201
C15	1.0pF	Cap cer 1pF 25V C0G/NP0	Murata	GJM0335C1E1R0BB0	C0201
C11	100PF	Cap cer 100PF 50V C0G/NP0	Murata	GRM0335C1H101JA01D	C0201
C14	1.5pF	Cap cer 1.5PF 50V C0G/NP0	Murata	GRM0335C1H1R5BA01D	C0201
C19	0.330nF	Cap cer 330PF 25V X7R	TDK	C0603X7R1E331M030BA	C0201
E1		Antenna 2.4~2.5GHz 50Ohm			
FB1	120 Ohms @ 100 MHz	Ferrite bead 120 Ohm 1LN	Murata	BLM03AG121SN1D	L0201
L1	10uH	Fixed 10uH 400mA 550MOhm	Microgate	MGFL1608F100MT-LF	L0603
L2	10nH	Fixed 10NH 500mA 350 MOhm	Murata	LQG15HN10NJ02D	L0402
L3	1.2nH	Fixed ind 1.2nH 600mA 150MOhm SM	Murata	LQP03TG1N2B02D	L0201
FB2	1kOhm@100MHz	Ferrite bead 1 kOhm	Murata	BLM15AG102SH1D	L0402
R1,L4	0Ohm	RES 0 Ohm jumper 1/20W	Bourns	CR0201-J/-000GLF	R0201
R2,R3	10K	Res SMD 10K Ohm 5% 1/10W	Panasonic	ERJ-2GEJ103X	R0402
TP1,TP2,TP3,TP4		Test Point			

Reference	Value	Description	Vendor	Part number	Foot print
U1	IN612L	IC SDR QFN6x6 48pins	InPlay	IN612L	QFN48
Y1	32.000 MHz	crystal 32 MHz 6pF SMD	NDK	NX1612SA-32.000MHZ-CHP-CIS-3	4-SMD
Y2	32.768 kHz	crystal 32.7680kHz 7pF SMD	ECS	ECS-.327-7-34B-C-TR	2-SMD

8. Layout

To ensure device performance, it is recommended to follow the general printed circuit board layout guidelines.

8.1. Layer stack-up

The recommendations in this document refer to the four-layer IN612L PCB based on standard flame retardant 4 (FR4) materials, a technology commonly used in commercial applications.

Table 25 : PCB layer stack-up

PCB Layer stack-up					
Layer	Purpose	Material	Thickness	Thickness control	Adjust to get desired total PCB thickness
Top layer +Plating	Signal	1/2 oz Cu	1.4	Yes	No
Dielectric		Roger 4003C	8	Yes	No
Internal Layer 1	GND	1/2 oz Cu	0.7	No	Yes
Dielectric		RF4	42	No	Yes
Internal Layer 1	Signal/power	1/2 oz Cu	0.7	No	Yes
Dielectric		RF4	8	No	Yes
Bottom Layer + Plating	Signal/power	1/2 oz Cu	1.4	No	Yes
		Total thickness	62		

8.2. Crystal

There is a high-speed 32MHz crystal in the system, the parasitic nature of the clock trace affects the oscillation, and the crystal should be placed as close as possible to the chip. Too wide traces can cause excessive capacitance, while too narrow traces can cause parasitic inductance of the clock traces. For short clock traces, use a trace width of approximately 10 mils (0.010 inches or 0.254 mm). Keep the crystal tuning capacitor close to the crystal pad.

Avoid passing through the crystal lines on adjacent layers. Keep the ground plane below the crystal line to improve the return path.

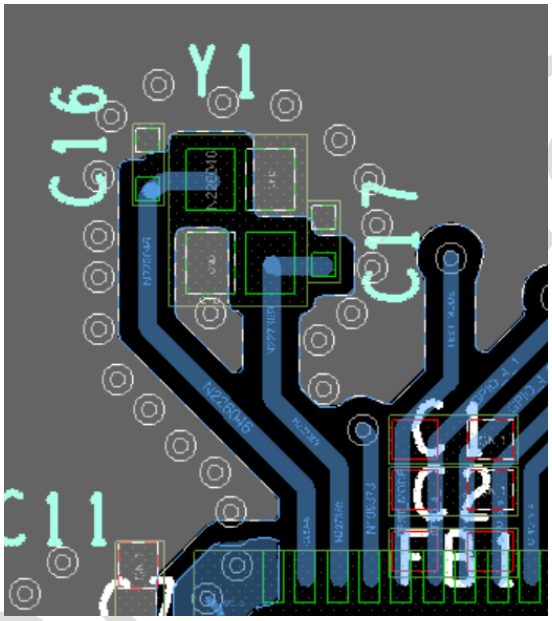


Figure 22 ： 32MHz crystal

The slow clock signal line must be as short as possible. The trace of the slow clock signal should have a ground plane on each side of the signal trace to reduce unwanted signal coupling. In order to reduce the capacitive coupling of unwanted signals to the clock line, the slow clock traces must not be higher or lower than other signals (especially digital signals).

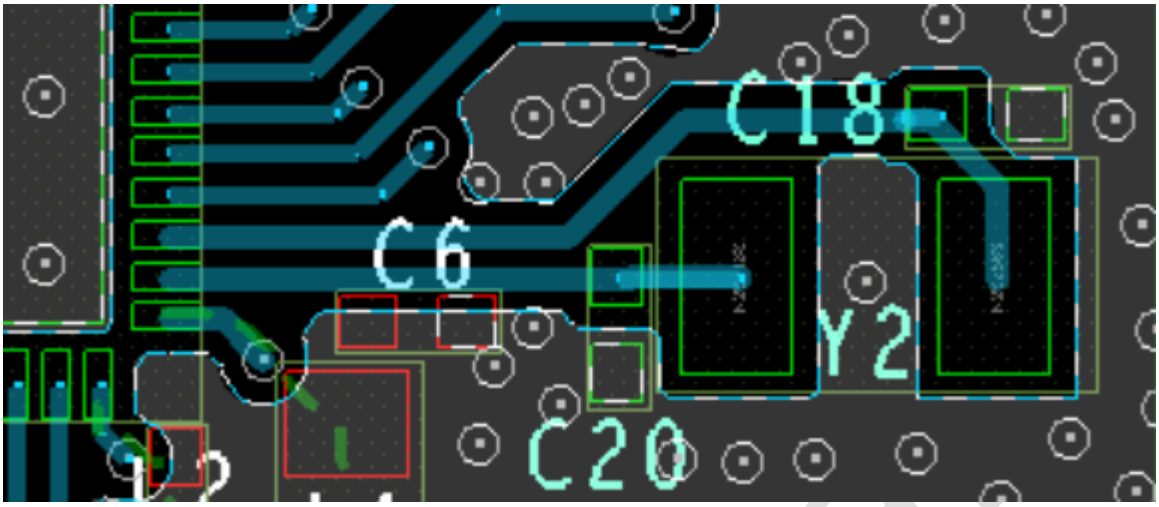


Figure 23 : 32.768KHz crystal

8.3. RF trace

Place the RF path on the top layer (component side) and keep the trace as short as possible. Referring to solid ground (Layer 2), the impedance of the RF trace must be controlled to 50 Ohms. In addition, ground Vias are required for better RF isolation.

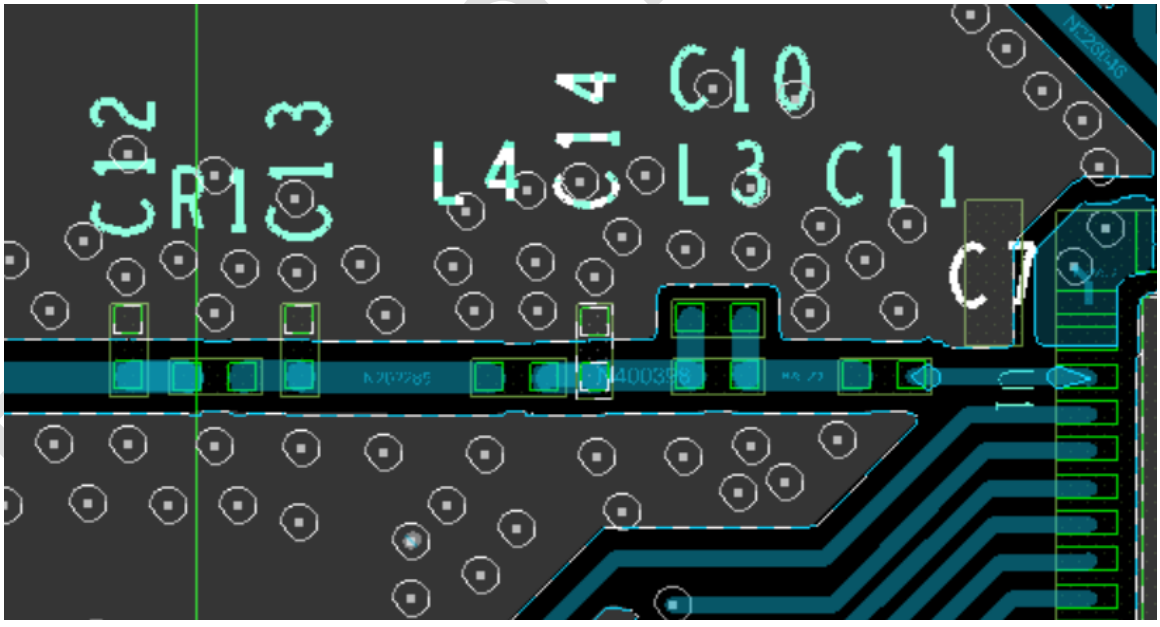


Figure 24 : RF trace

8.4. Antenna

Antenna is a key component in wireless system design to make sure the device will perform as expected. Make sure to select the antenna that covers the appropriate frequency band from 2.350GHz to 2.550GHz. Talk to the antenna supplier and make sure he understands that the antenna must cover the entire frequency range. Also make sure the antenna is designed for a 50Ω impedance system. Make sure the PCB pads to which the antenna is connected are properly designed to have a 50Ω impedance. The antenna supplier must specify the pad size, the pitch from the pad to the ground reference plane, and the spacing from the pad edge to the ground fill on the same layer as the pad. In addition, since the ground reference plane from the antenna pad to the 50Ω trace of the IN6I2NL may be on a different layer than the ground reference of the antenna pad, ensure that the pad design has an appropriate transition from pad to pad 50Ω trace. Make sure the antenna matching components are placed as close as possible to the antenna pads. Always consult with an antenna expert on antenna matching to ensure the best RF performance.

8.5. PMU LDO output

Shorter trace lengths should be used to avoid overload. The 1.2V output needs to be fully filtered through 4.7uf capacitor, then connect to the DCDC & RF power pins, The bigger inductor should use the low DRC winding inductor.

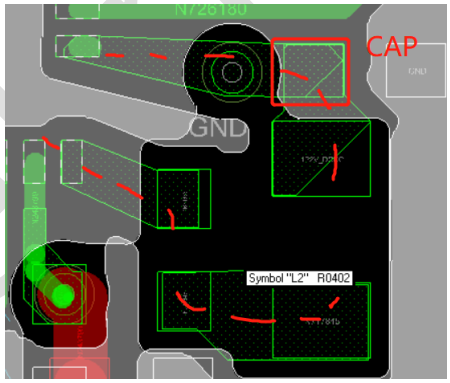


Figure 25 ：IP2V-DCDC output

Note that the PMU is a switching regulator that produces noise in the 2.4 GHz receive band. Therefore, RF routing, components and antennas must be as far as possible from the PMU and its components (L1, L2 and C6).

8.6. VBAT power supply

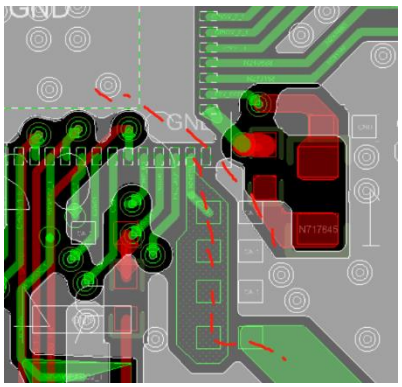


Figure 26 : VBAT trace

The VBAT power supply is same as LDO 1.2V output. This is the power supply for the PMU, and the noise of the PMU is fed back to the power supply pin. FB2 is used to suppress noise and prevent it from radiating from the power supply path. Therefore, the RF path should also be kept away from the VBAT supply path and FB2, C3, C4 and C16.

The filter capacitor on the VBAT pin needs to be as close as possible, and the ground pads of the capacitors need to be close to the chip ground, This is very important for internal RC clock.

8.7. Power supply

Below routing requirements for power supplies shall apply to the IN612L device:

- Short power supply trace length
- Decoupling capacitor placed as close as possible to the device
  - C7 close to VDD_RF_2G4
  - C9 close to VDDIO2
  - C8 close to VDDIO1
  - C1 and C2 close to VDD_AMS

The most common ground loop problem occurs when the ground loop current has a longer return path due to placing the DC bypass capacitor to ground.

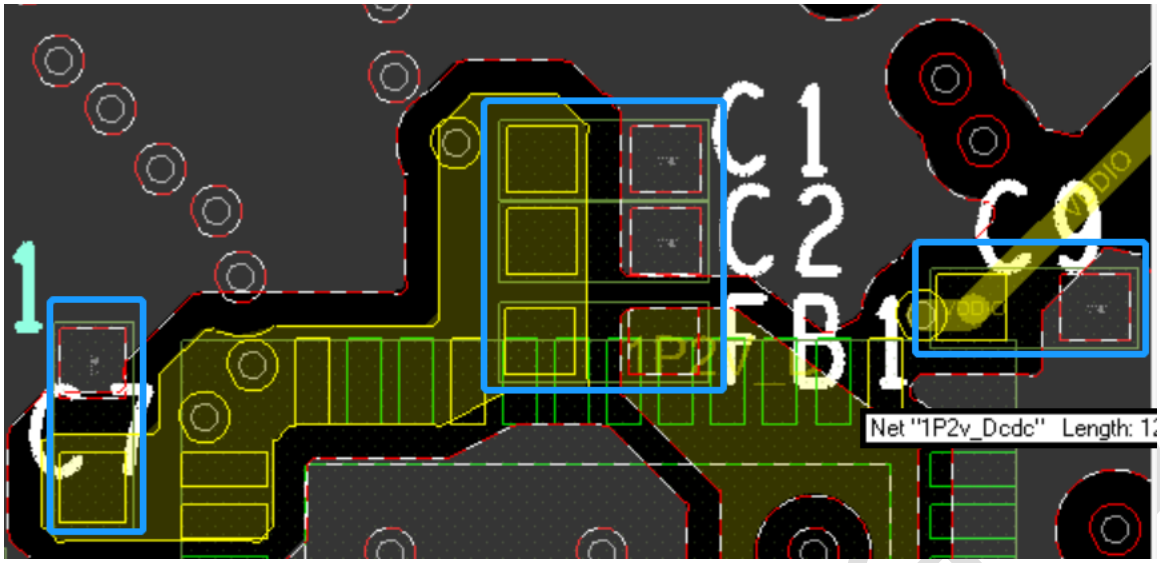


Figure 27 : Placement with RF power routing

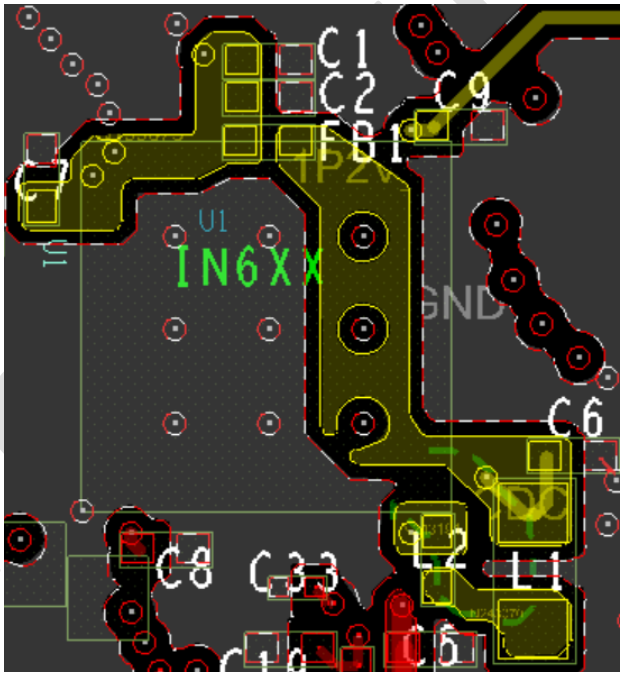


Figure 28 : Routing of 1P2V supply

8.8. Thermal pad VIAs

To increase the ground coupling, add at least 9 Vias directly to the SoC's thermal pad to the solid ground, as shown in *Figure 29*.

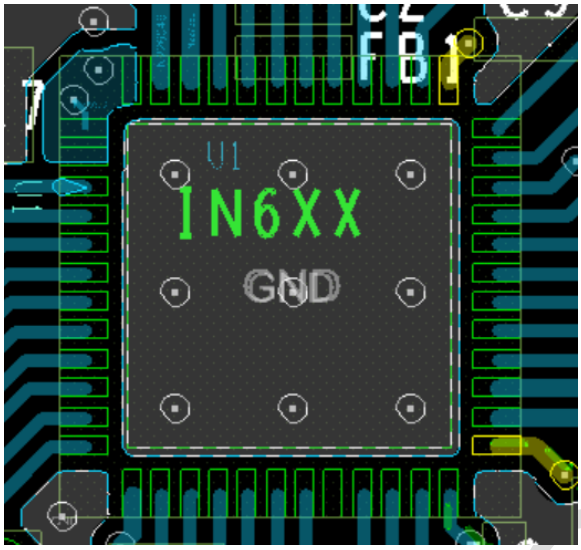


Figure 29 : Thermal pad vias

8.9. Ground

Use a dedicated one layer for the ground plane. Make sure this ground plane is not broken down by the route. The power supply can be routed on all layers except the ground floor. The power path should be a heavy copper filled plane to ensure the lowest possible inductance.

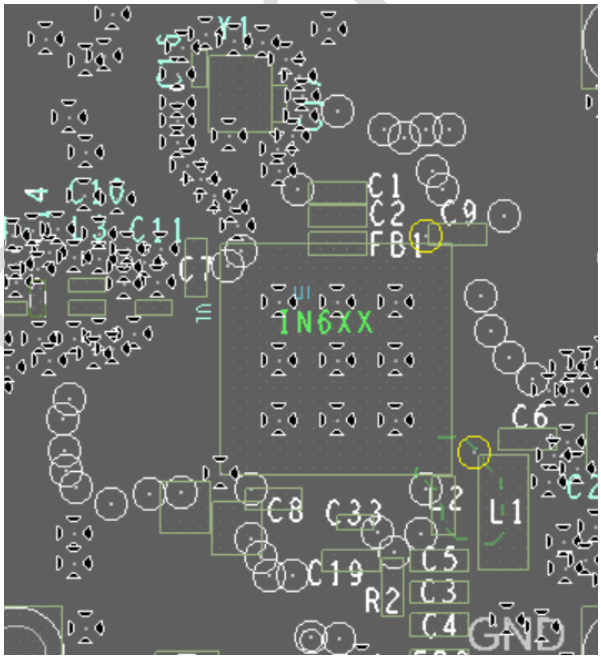


Figure 30 : Example of ground layer

9. Reflow Profile Information

This section provides guidelines for reflow processes in getting the InPlay Device soldered to the user's design.

9.1. Storage condition

9.1.1. Moisture barrier bag before opened

A moisture barrier bag must be stored in a temperature of less than 30°C with humidity under 85% RH. The calculated shelf life for the dry-packed product shall be 12 months from the date the bag is sealed.

9.1.2. Moisture barrier bag open

Humidity indicator cards must be blue, < 30%.

9.2. Stencil design

The recommended stencil is laser-cut, stainless-steel type with a thickness of 100μm to 130μm and approximately a 1:1 ratio of stencil opening to pad dimension. To improve paste release, a positive taper with bottom opening 25μm larger than the top can be utilized. Local manufacturing experience may find other combinations of stencil thickness and aperture size to get good results.

9.3. Baking conditions

This module is rated at MSL level 3. After sealed bag is opened, no baking is required within 168 hours so long as the devices are held at <= 30°C /60% RH or stored at <10% RH.
The module will require baking before mounting if:
The sealed bag has been open for > 168 hours.
Humidity Indicator Card reads >10%.
SIPs need to be baked for 8 hours at 125°C.

9.4. Soldering and reflow condition

9.4.1. Reflow oven

It is strongly recommended that a reflow oven equipped with more heating zones and Nitrogen atmosphere be used for lead-free assembly. Nitrogen atmosphere has shown to improve the wet-ability and reduce temperature gradient across the board. It can also enhance the appearance of the solder joints by reducing the effects of oxidation.
The following items should also be observed in the reflow process:

1. Some recommended pastes include NC-SMQ® 230 flux and Indalloy® 241 solder paste made up of 95.5 Sn/3.8 Ag/0.7 Cu or SENJU N705-GRN3360-K2-V type 3, no clean paste.
2. Allowable reflow soldering times: Three times based on the following reflow soldering profile (as shown in *Figure 31*).
3. Temperature profile: Reflow soldering shall be done according to the following temperature profile (as shown in *Figure 31*).
4. Peak temperature: 250°C.

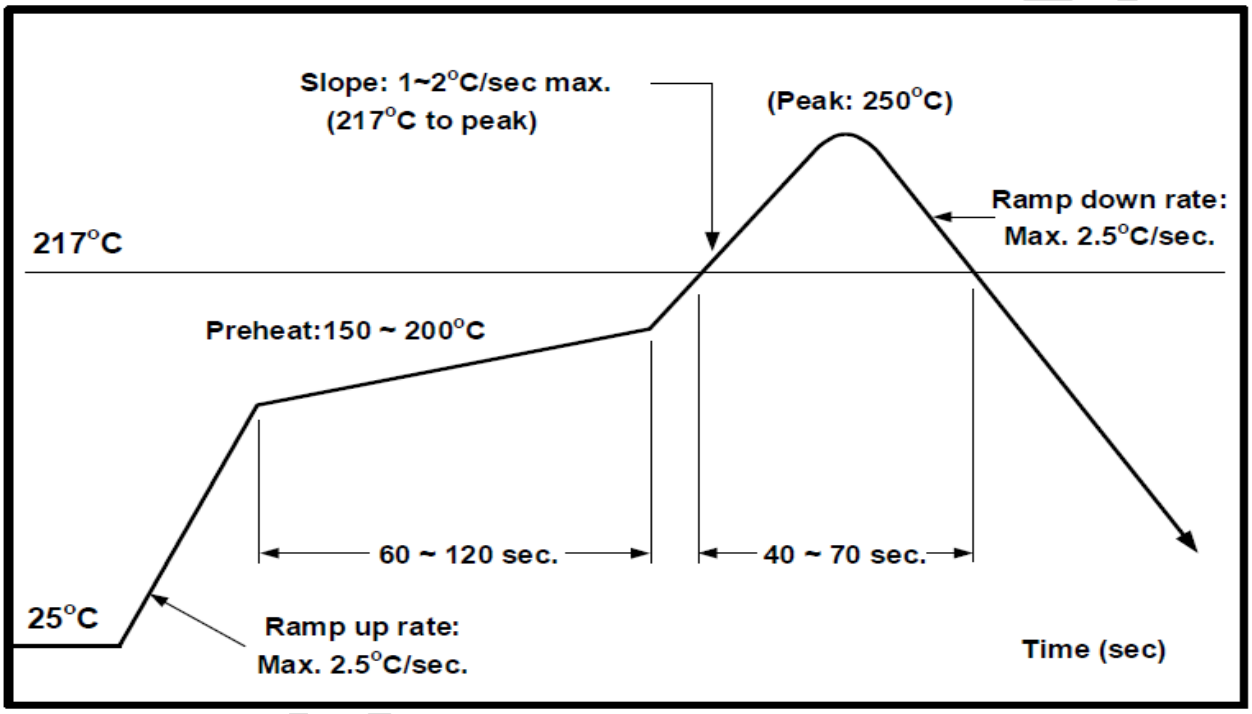


Figure 31 : Solder reflow profile

10. Revision History

Revision	Description	Date	Drafted by
V1.0	Initial Version	6/30/2020	
V1.10	Modify the document format	03/21/2022	

11. Disclaimer

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