PCN Number: 201			180308002-001			PCN I	CN Date: Mar 26, 2018		Mar 26, 2018	
Title: Transfer of select \			VIP3	/IP3 devices from GFAB to DFAB Wafer Fab site						
Customer Contact:				PCN Manager			Dept:			Quality Services
Proposed 1 st Ship Date:				Sep	26, 2018	Estimated Sample Availability:		Date provided at sample request.		
Change Type:										
Assembly Site			Assembly Process				Assembly Materials			
Design			☐ Electrical Specification					Me	chanical Specification	
Test Site			Packing/Shipping/Labeling					Tes	st Process	
☐ Wafer Bump Site			Wafer Bump Material					Wa	fer Bump Process	
							Wa	fer Fab Process		
				Part number change						
	PCN Details									

Description of Change:

This change notification is to announce the transfer of select VIP3 devices from GFAB to the DFAB (DL-LIN) Wafer Fab site for the selected devices listed in the "Product Affected" section.

	Current Fab Site		New Fab Site			
Current Fab Site	Process	Wafer Diameter	New Fab Site	Process	Wafer Diameter	
GFAB6	VIP3	150 mm	DL-LIN	VIP3	200 mm	

Qual details are provided in the Qual Data Section.

Reason for Change:

Greenock, Scotland (GFAB) Wafer Fab site closure

Anticipated impact on Form, Fit, Function, Quality or Reliability (positive / negative):

None

Changes to product identification resulting from this PCN:

Current:

Current Chip Site	Chip Site Origin Code (20L)	Chip Site Country Code (21L)	Chip Site City
GFAB6	GF6	GBR	Greenock

New Fab Site:

New Chip Site	Chip Site Origin Code (20L)	Chip Site Country Code (21L)	Chip Site City
DL-LIN	DLN	USA	Dallas

Sample product shipping label (not actual product label)





(1P) SN74LS07NSR (D) 0336 31T)LOT: 3959047MLA 4W) TKY(1T) 7523483S12 (20L) CSO: SHE (21L) CCO:USA (22L) ASO: MLA (23L) ACO: MA

Product Affected:

LM7321QMF/NOPB	LM7321QMFX/NOPB	LM7322QMA/NOPB	LM7322QMAX/NOPB
LM7321QMFE/NOPB			

Automotive New Product Qualification Summary

(As per AEC-Q100 and JEDEC Guidelines)

VIP3 Qualification at DFAB Approved 06-Mar-2018

Product Attributes

Attributes	Qual Device: LM6172IM/NOPB			
Operating Temp Range	-			
Automotive Grade Level	-			
Product Function	Feedback Amplifier			
Wafer Fab Supplier	DFAB 200MM			
Wafer Process	VIP3			
Die Revision	С			
Assembly Site	TIEMA			
Package Type	SOIC			
Package Designator	D			
Ball/Lead Count	8			

⁻ Qual Devices qualified at LEVEL1-260CG: LM6172IM/NOPB

Qualification Results

Data Displayed as: Number of lots / Total sample size / Total failed

	Data Displayed as: Number of lots / Total sample size / Total failed							
	Туре	#	Test Spec	Min Lot Qty	SS/ Lot	Test Name / Condition	Duration	Qual Device: LM6172IM/NOPB
Te	Test Group A – Accelerated Environment Stress Tests							
	HAST	A2	JEDEC JESD22-A110	3	77	Biased HAST, 130C/85%RH	96 Hours	3/231/0
	AC	А3	JEDEC JESD22-A102	3	77	Autoclave 121C	96 Hours	3/231/0
	тс	A4	JEDEC JESD22-A104 and Appendix 3	3	77	Temperature Cycle, -65/150C	500 Cycles	3/231/0
	TC-BP	C2	MIL-STD883 Method 2011	1	30	Post Temp. Cycle Bond Pull	500 Cycles	3/15/0
	PTC	A5	JEDEC JESD22-A105	1	45	Power Temperature Cycle	1000 Cycles	N/A
	HTSL	A6	JEDEC JESD22-A103	1	45	High Temp Storage Bake 150C	1000 Hours	3/231/0
T	est Group B –	Acce	lerated Lifetime Simulation	Tests				
	HTOL	B1	JEDEC JESD22-A108	3	77	Life Test, 125C	1000 Hours	3/231/0
	ELFR	B2	AEC Q100-008	3	800	Early Life Failure Rate, 125C	48 Hours	3/2400/0
	EDR	В3	AEC Q100-005	3	77	NVM Endurance, Data Retention, and Operational Life	-	N/A
T	est Group C –	Pack	age Assembly Integrity Test	5				
	WBS	C1	AEC Q100-001	1	30	Bond Shear (Cpk>1.67)	Wires	1/30/0
	WBP	C2	MIL-STD883 Method 2011	1	30	Bond Pull (Cpk>1.67)	Wires	1/30/0
	SD	СЗ	JEDEC JESD22-B102	1	15	Surface Mount Solderability >95% Lead Coverage	Pb & Pb-Free	1/30/0
	PD	C4	JEDEC JESD22-B100 and B108	3	10	Physical Dimensions (Cpk>1.67)	-	3/30/0
	SBS	C5	AEC Q100-010	3	50	Solder Ball Shear (Cpk>1.67)	Post HTSL/Bump	N/A
Te	est Group D –	Die F	abrication Reliability Tests					
Г	EM	D1	JESD61	-	-	Electromigration	-	Completed Per Process Technology Requirements
	TDDB	D2	JESD35	-	-	Time Dependant Dielectric Breakdown	-	Completed Per Process Technology Requirements
	HCI	D3	JESD60 & 28	-	-	Hot Injection Carrier	1	Completed Per Process Technology Requirements
	NBTI	D4	-	-	-	Negative Bias Temperature Instability	1	Completed Per Process Technology Requirements
	SM	D5	-	-	-	Stress Migration	ı	Completed Per Process Technology Requirements
T	Test Group E – Electrical Verification Tests							
	ED	E5	AEC Q100-009	3	30	Electrical Distributions	Cpk>1.67 Room, Hot, & Cold	3/90/0
A	dditional Test	ts						
	MΩ			-	-	Manufacturability (Auto Assembly)	(per automotive requirements)	3/Pass
	MΩ			-	-	Manufacturability (Wafer Fab)	(per mfg. Site specification)	3/Pass

A1 (PC): Preconditioning:

Performed for THB, Biased HAST, AC, uHAST, TC & PTC samples, as applicable.

Ambient Operating Temperature by Automotive Grade Level:

Grade 0 (or E): -40°C to +150°C Grade 1 (or Q): -40°C to +125°C Grade 2 (or T): -40°C to +105°C Grade 3 (or I): -40°C to +85°C

E1 (TEST): Electrical test temperatures of Qual samples (High temperature according to Grade level):

Room/Hot/Cold : HTOL, ED

Room/Hot: THB / HAST, TC / PTC, HTSL, ELFR, ESD & LU

Room: AC/uHAST Green/Pb-free Status:

Qualified Pb-Free(SMT) and Green

For questions regarding this notice, e-mails can be sent to the regional contacts shown below, or you can contact your local Field Sales Representative.

Location	E-Mail
USA	PCNAmericasContact@list.ti.com
Europe	PCNEuropeContact@list.ti.com
Asia Pacific	PCNAsiaContact@list.ti.com
Japan	PCNJapanContact@list.ti.com