LM25066A System Power Management and Protection IC With PMBus™

1 Features

- Input Voltage Range: 2.9 V to 17 V
- I^2C/SMBus Interface and PMBus Compliant Command Structure
- Programmable 25-mV or 46-mV Current Limit Threshold
- Configurable Circuit Breaker Protection for Hard Shorts
- Configurable Undervoltage and Overvoltage Lockouts With Hysteresis
- Remote Temperature Sensing With Programmable Warning and Shutdown Thresholds
- Detection and Notification of Damaged MOSFET Condition
- Real Time Monitoring of V_{IN}, V_{OUT}, I_{IN}, P_{IN}, V_{AUX} With 12-Bit Resolution and 1-kHz Sampling Rate
- Current Measurement Accuracy: ±1% Over Temperature
- Power Measurement Accuracy: ±2% Over Temperature
- True Input Power Measurement Using Simultaneous Sampling of V_{IN} and I_{IN} Accurately Averages Dynamic Power Readings
- Averaging of V_{IN}, I_{IN}, P_{IN}, and V_{OUT} Over Programmable Interval Ranging from 0.001 to 4 Seconds
- Programmable WARN and FAULT Thresholds with $\overline{SMBA}$ Notification
- Black Box Capture of Telemetry Measurements and Device Status Triggered by WARN or FAULT Condition
- 24-Lead WQFN Package

2 Applications

- Server Backplane Systems
- Basestation Power Distribution Systems
- Solid State Circuit Breakers

3 Description

The LM25066A combines a high-performance hot-swap controller with a PMBus™ compliant SMBus/I^2C interface to accurately measure, protect and control the electrical operating conditions of computing and storage blades connected to a backplane power bus. The LM25066A continuously supplies real-time power, voltage, current, temperature and fault data to the system management host via the SMBus interface.

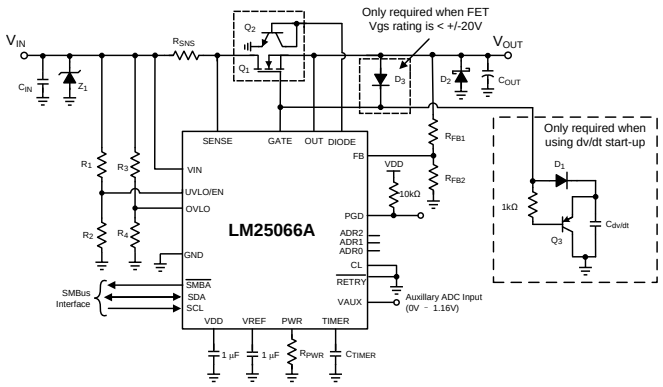
The LM25066A control block includes a unique hot-swap architecture that provides current and power limiting to protect sensitive circuitry during insertion of boards into a live system backplane, or any other *hot* power source. A fast acting circuit breaker prevents damage in the event of a short circuit on the output. The input undervoltage and overvoltage levels and hysteresis are configurable, as well as the insertion delay time and fault detection time. A temperature monitoring block on the LM25066A interfaces with a low-cost external diode for monitoring the temperature of the external MOSFET or other thermally sensitive components. The POWER GOOD output provides a fast indicator when the input and/or output voltages are outside their programmed range. LM25066A current measurement accuracy is ±1% over temperature.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LN25066A	WQFN (24)	5.00 mm × 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (February 2013) to Revision G — **Page**

- Added *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* ... 1

Changes from Revision E (February 2013) to Revision F — **Page**

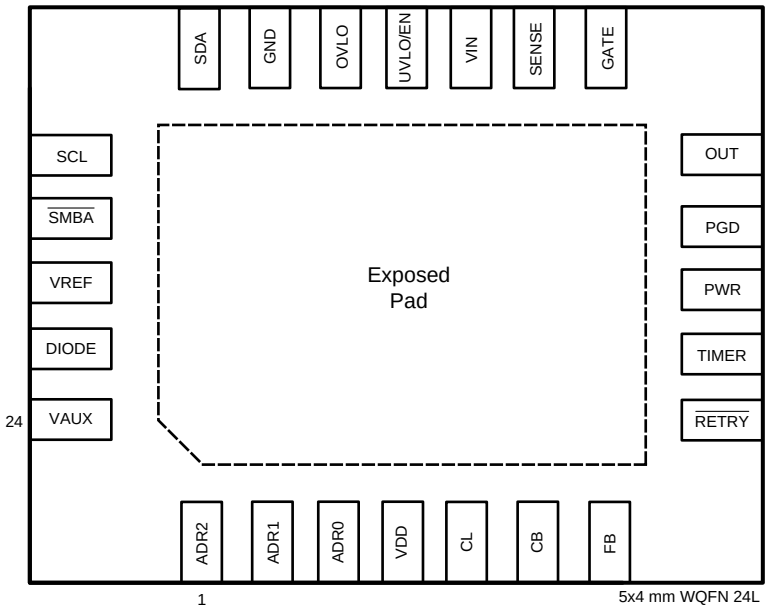
- Changed layout of National Semiconductor Data Sheet to TI format ... 1

5 Description (continued)

The LM25066A monitoring block computes both the real-time and average values of subsystem operating parameters (V_{IN}, I_{IN}, P_{IN}, V_{OUT}) as well as the peak power. Accurate power averaging is accomplished by averaging the product of the input voltage and current. A black box (Telemetry/Fault Snapshot) function captures and stores telemetry data and device status in the event of a warning or a fault.

6 Pin Configuration and Functions

NHZ Package
24-Pin WQFN
Top View



Solder the exposed pad to ground.

Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	ADR2	SMBUS address line 2	3 - state address line. Should be connected to GND, VDD, or left floating.
2	ADR1	SMBUS address line 1	3 - state address line. Should be connected to GND, VDD, or left floating.
3	ADR0	SMBUS address line 0	3 - state address line. Should be connected to GND, VDD, or left floating.
4	VDD	Internal sub-regulator output	Internally sub-regulated 4.5-V bias supply. Connect a 1-µF capacitor on this pin to ground for bypassing.
5	CL	Current limit range	Connect this pin to GND to set the nominal overcurrent threshold at 25 mV. Connecting CL to VDD sets the overcurrent threshold to be 46 mV.
6	CB	Circuit breaker range	This pin sets the circuit breaker protection point in relation to the overcurrent trip point. When connected to GND, this pin sets the circuit breaker point to be 1.8 times the overcurrent threshold. Connecting this pin to VDD sets the circuit breaker trip point to be 3.6 times the overcurrent threshold.
7	FB	Power Good feedback	An external resistor divider from OUT sets the output voltage at which the PGD pin switches. The threshold at the pin is 1.167 V. An internal 24-µA current source provides hysteresis.
8	$\overline{\text{RETRY}}$	Fault retry input	This pin configures the power up fault retry behavior. When this pin is grounded, the device continually tries to engage power during a fault. If the pin is connected to VDD, the device will latch off during a fault.
9	TIMER	Timing capacitor	An external capacitor connected to this pin sets the insertion time delay, fault timeout period and restart timing.
10	PWR	Power limit set	An external resistor connected to this pin, in conjunction with the current sense resistor (R_S), sets the maximum power dissipation allowed in the external series pass MOSFET.

Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NO.	NAME		
11	PGD	Power Good indicator	An open drain output. This output is high when the voltage at the FB pin is above 1.167 V and the input supply is within its undervoltage and overvoltage thresholds. Connect through a pullup resistor to the output rail (external MOSFET source) or any other voltage to be monitored.
12	OUT	Output feedback	Connect to the output rail (external MOSFET source). Internally used to determine the MOSFET V_{DS} voltage for power limiting, and to monitor the output voltage.
13	GATE	Gate drive output	Connect to the external MOSFET's gate.
14	SENSE	Current sense input	The voltage across the current sense resistor (R_S) is measured from VIN to this pin. If the voltage across R_S reaches overcurrent threshold, the load current is limited and the fault timer activates.
15	VIN	Positive supply input	A small ceramic bypass capacitor close to this pin is recommended to suppress transients which occur when the load current is switched off.
16	UVLO/EN	Under-voltage lockout	An external resistor divider from the system input voltage sets the undervoltage turnon threshold. An internal 23-µA current source provides hysteresis. The enable threshold at the pin is 1.16 V. This pin can also be used for remote shutdown control.
17	OVLO	Over-voltage lockout	An external resistor divider from the system input voltage sets the overvoltage turnoff threshold. An internal 23-µA current source provides hysteresis. The disable threshold at the pin is 1.16 V.
18	GND	Circuit ground	
19	SDA	SMBus data pin	Data pin for SMBus.
20	SCL	SMBus clock	Clock pin for SMBus.
21	$\overline{\text{SMBA}}$	SMBus alert line	Alert pin for SMBus, active low.
22	VREF	Internal Reference	Internally generated precision 2.73-V reference used for analog to digital conversion. Connect a 1-µF capacitor on this pin to ground for bypassing.
23	DIODE	External diode	Connect this to a diode-configured NPN transistor for temperature monitoring.
24	VAUX	Auxiliary voltage input	Auxiliary pin allows voltage telemetry from an external source. Full scale input of 1.16 V.
Pad	Exposed Pad	Exposed pad of WQFN package	No internal electrical connections. Solder to the ground plane to reduce thermal resistance.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Input voltage	VIN, SENSE to GND (2)	–0.3	24	V
	GATE, FB, UVLO/EN, OVLO, PGD to GND (2)	–0.3	20	V
	OUT to GND	–1	20	V
	SCL, SDA, $\overline{\text{SMBA}}$, CL, CB, ADR0, ADR1, ADR2, VDD, VAUX, DIODE, $\overline{\text{RETRY}}$ to GND	–0.3	6	V
	VIN to SENSE	–0.3	0.3	V
Junction Temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The GATE pin voltage is typically 7.5 V above VIN when the LM25066A is enabled. Therefore the Absolute Maximum Rating of 24 V for VIN and SENSE apply only when the LM25066A is disabled or for a momentary surge to that voltage since the Absolute Maximum Rating of the GATE pin is 20V.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM) (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±500	

(1) The human body model is a 100-pF capacitor discharged through a 1.5 kΩ resistor into each pin.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
VIN, SENSE, OUT voltage	2.9		17	V
VDD	2.9		5.5	V
Junction temperature, T_J	–40		125	°C

7.4 Thermal Information

THERMAL METRIC (1)		LM25066A NHZ (WQFN) 24 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	34.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	28.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	13.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	13.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

Typical limits are for T_J = 25°C, and minimum and maximum limits apply over the operating junction temperature range (–40°C to 85°C). Minimum and Maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: VIN = 12 V.(1)(2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT (VIN PIN)						
I_{IN-EN}	Input current, enabled	UVLO = 2 V and OVLO = 0.7 V		5.8	8	mA
POR	Power on reset threshold at VIN	VIN increasing		2.6	2.8	V
POR_{HYS}	POR_{EN} hysteresis	VIN decreasing		150		mV
VDD REGULATOR (VDD PIN)						
V_{DD}		I_{VDD} = 5 mA, VIN = 12 V	4.3	4.5	4.7	V
		I_{VDD} = 5 mA, VIN = 4.5 V	3.5	3.9	4.3	V
V_{DDILIM}	VDD current limit		25	45		mA
UVLO/EN, OVLO PINS						
$UVLO_{TH}$	UVLO threshold	V_{UVLO} Falling	1.147	1.16	1.173	V
$UVLO_{HYS}$	UVLO hysteresis current	UVLO = 1 V	18	23	28	µA
$UVLO_{DEL}$	UVLO delay	Delay to GATE high		8		µs
		Delay to GATE low		20		
$UVLO_{BIAS}$	UVLO bias current	UVLO = 3 V			1	µA
$OVLO_{TH}$	OVLO threshold	V_{OVLO} rising	1.141	1.16	1.185	V
$OVLO_{HYS}$	OVLO hysteresis current	OVLO = 1 V	–28	–23	–18	µA
$OVLO_{DEL}$	OVLO delay	Delay to GATE high		19		µs
		Delay to GATE low		9		
$OVLO_{BIAS}$	OVLO bias current	OVLO = 1 V			1	µA
POWER GOOD (PGD PIN)						
PGD_{VOL}	Output low voltage	I_{SINK} = 2 mA		25	60	mV
PGD_{IOH}	Off leakage current	V_{PGD} = 17 V			1	µA
PGD_{DELAY}	Power Good delay	V_{FB} to V_{PG}		115		ns
FB PIN						
FB_{TH}	FB threshold	V_{FB} rising	1.141	1.167	1.19	V
FB_{HYS}	FB hysteresis current		–31	–24	–18	µA
FB_{LEAK}	Off leakage current	V_{FB} = 1 V			1	µA
POWER LIMIT (PWR PIN)						
PWR_{LIM}	Power limit sense voltage (VIN-SENSE)	SENSE-OUT = 12 V, R_{PWR} = 25 kΩ	9	12.5	15	mV
I_{PWR}	PWR pin current	V_{PWR} = 2.5 V		–10		µA
$R_{SAT(PWR)}$	PWR pin impedance when disabled	UVLO = 0.7 V		180		Ω
GATE CONTROL (GATE PIN)						
I_{GATE}	Source current	Normal operation	–28	–22	–16	µA
	Fault sink current	UVLO = 1 V	1.5	2	2.5	mA
	POR circuit breaker sink current	VIN - SENSE = 150 mV or VIN < R_{POR}, V_{GATE} = 5 V	105	190	275	mA
V_{GATE}	Gate output voltage in normal operation	GATE voltage with respect to ground	17	18.8	20.3	V
OUT PIN						
I_{OUT-EN}	OUT bias current, enabled	OUT = VIN, normal operation		16		µA
$I_{OUT-DIS}$	OUT bias current, disabled(3)	Disabled, OUT = 0 V, SENSE = VIN		–12		µA

(1) Current out of a pin is indicated as a negative value.
(2) All electrical characteristics having room temperature limits are tested during production at T_A = 25°C. All hot and cold limits are specified by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(3) OUT bias current (disabled) due to leakage current through an internal 0.9 MΩ resistance from SENSE to VOUT.

Electrical Characteristics (continued)

Typical limits are for T_J = 25°C, and minimum and maximum limits apply over the operating junction temperature range (–40°C to 85°C). Minimum and Maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: VIN = 12 V.(1)(2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT LIMIT						
V_{CL}	Threshold voltage	CL = GND	22.5	25	27	mV
		CL = GND, T_J = 10°C to 85°C	23	25	27	
		CL = VDD	42.3	46	49.7	
I_{SENSE}	SENSE input current	Enabled, SENSE = OUT		33		µA
		Disabled, OUT = 0 V		46		
		Enabled, OUT = 0 V		45		
CIRCUIT BREAKER						
V_{CB}	Threshold voltage × 1.8	VIN - SENSE, CL = GND, CB = GND	35	45	55	mV
	CB:CL ratio	CB = GND	1.6	1.8	2	
V_{CB}	Threshold voltage × 3.6	VIN - SENSE, CL = GND, CB = VDD	70	90	110	mV
	CB:CL ratio	CB = VDD	3.1	3.6	4	
TIMER (TIMER PIN)						
V_{TMRH}	Upper threshold		1.54	1.7	1.85	V
V_{TMRL}	Lower threshold	Restart cycles	0.85	1	1.07	V
		End of 8th cycle		0.3		V
		Re-enable threshold		0.3		V
I_{TIMER}	Insertion time current	TIMER pin = 2 V	–3	–5.5	–8	µA
	Sink current, end of insertion time		1.4	1.9	2.4	mA
	Fault detection current		–120	–90	–60	µA
	Fault sink current			2.8		µA
DC_{FAULT}	Fault restart duty cycle			0.67%		
INTERNAL REFERENCE						
V_{REF}	Reference voltage		2.703	2.73	2.757	V
ADC AND MUX						
	Resolution			12		Bits
INL	Integral non-linearity	ADC only		±1		LSB
TELEMETRY ACCURACY						
IIN_{FSR}	Current input full scale range	CL = GND		30.2		mV
		CL = VDD		60.4		mV
IIN_{LSB}	Current input LSB	CL = GND		7.32		µV
		CL = VDD		14.64		µV
$VAUX_{FSR}$	VAUX input full scale range			1.16		V
$VAUX_{LSB}$	VAUX input LSB			283.2		µV
VIN_{FSR}	Input voltage full scale range			18.7		V
VIN_{LSB}	Input voltage LSB			4.54		mV
IIN_{ACC}	Input current accuracy	VIN – SENSE = 25 mV, CL = GND	–1.2%		1%	
		VIN – SENSE = 25 mV, CL = GND T_J = 10°C to 85°C	–1%		1%	
		VIN – SENSE = 50 mV, CL = VDD	–1.8%		1.8%	
		VIN – SENSE = 50 mV, CL = GND T_J = 10°C to 85°C	–5%		5%	

Electrical Characteristics (continued)

Typical limits are for T_J = 25°C, and minimum and maximum limits apply over the operating junction temperature range (–40°C to 85°C). Minimum and Maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: VIN = 12 V.(1)(2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{ACC}	VAUX, VIN, VOUT accuracy	VIN, VOUT = 12 V VAUX = 1 V	–1%		1.2%	
		VIN, VOUT = 12 V VAUX = 1 V T_J = 10°C to 85°C	–1%		1%	
PIN_{ACC}	Input power accuracy	VIN = 12 V, VIN – SENSE = 25 mV, CL = GND	–2.3%		2%	
		VIN = 12 V, VIN – SENSE = 25 mV, CL = GND, T_J = 10°C to 85°C	–2%		2%	
REMOTE DIODE TEMPERATURE SENSOR						
T_{ACC}	Temperature accuracy using local diode	T_A = 10°C to 85°C		2	10	°C
	Remote diode resolution			9		bits
I_{DIODE}	External diode current source	High level		250	300	µA
		Low level		9.4		µA
	Diode current ratio			26		
PMBUS PIN THRESHOLDS ($\overline{SMBA}$, SDA, SCL)						
V_{IL}	Data, clock input low voltage				0.8	V
V_{IH}	Data, clock input high voltage		2.1		5.5	V
V_{OL}	Data output low voltage	I_{PULLUP} = 500 µA	0		0.4	V
I_{LEAK}	Input leakage current	SDA, $\overline{SMBA}$, SCL = 5 V			1	µA
CONFIGURATION PIN THRESHOLDS (CB, CL, $\overline{RETRY}$)						
V_{IH}	Threshold voltage		3			V
I_{LEAK}	Input leakage current	CL, CB, $\overline{RETRY}$ = 5 V			1	mA

7.6 Timing Requirements: SMBus Communications

		MIN	MAX	UNIT
F_{SMB}	SMBus Operating Frequency	10	400	kHz
T_{BUF}	Bus free time between Stop and Start Condition	1.3		µs
$T_{HD:STA}$	Hold time after (Repeated) Start Condition. After this period, the first clock is generated.	0.6		µs
$T_{SU:STA}$	Repeated Start Condition setup time	0.6		µs
$T_{SU:STO}$	Stop Condition setup time	0.6		µs
$T_{HD:DAT}$	Data hold time	300		ns
$T_{SU:DAT}$	Data setup time	100		ns
$T_{TIMEOUT}$	Clock low timeout(1)	25	35	ms
T_{LOW}	Clock low period	1.5		µs
T_{HIGH}	Clock high period(2)	0.6		µs
$T_{LOW:SEXT}$	Cumulative clock low extend time (slave device)(3)		25	ms
$T_{LOW:MEXT}$	Cumulative low extend time (master device)(4)		10	ms
T_F	Clock or Data Fall Time(5)	20	300	ns
T_R	Clock or Data Rise Time(5)	20	300	ns

(1) Devices participating in a transfer will timeout when any clock low exceeds the value of $T_{TIMEOUT,MIN}$ of 25 ms. Devices that have detected a timeout condition must reset the communication no later than $T_{TIMEOUT,MAX}$ of 35 ms. The maximum value must be adhered to by both a master and a slave as it incorporates the cumulative stretch limit for both a master (10ms) and a slave (25ms).
(2) $T_{HIGH\ MAX}$ provides a simple method for devices to detect bus idle conditions.
(3) $T_{LOW:SEXT}$ is the cumulative time a slave device is allowed to extend the clock cycles in one message from the initial start to the stop. If a slave exceeds this time, it is expected to release both its clock and data lines and reset itself.
(4) $T_{LOW:MEXT}$ is the cumulative time a master device is allowed to extend its clock cycles within each byte of a message as defined from start-to-ack, ack-to-ack, or ack-to-stop.
(5) Rise and fall time is defined as follows: T_R = (V_{ILMAX} – 0.15) to (V_{IHMIN} + 0.15) x T_F = 0.9 VDD to (V_{ILMAX} – 0.15)

7.7 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
CURRENT LIMIT							
t_{CL}	Response time	VIN-SENSE stepped from 0 mV to 80 mV			1.2		µs
CIRCUIT BREAKER							
t_{CB}	Response time	VIN - SENSE stepped from 0 mV to 150 mV, time to GATE low, no load	T_J = –40°C to 85°C		0.6	1.2	µs
TIMER (TIMER PIN)							
t_{FAULT_DELAY}	Fault to GATE low delay	TIMER pin reaches the upper threshold			17		µs
ADC AND MUX							
t_{AQUIRE}	Acquisition + Conversion Time	Any channel			100		µs
t_{RR}	Acquisition Round Robin Time	Cycle all channels			1		ms

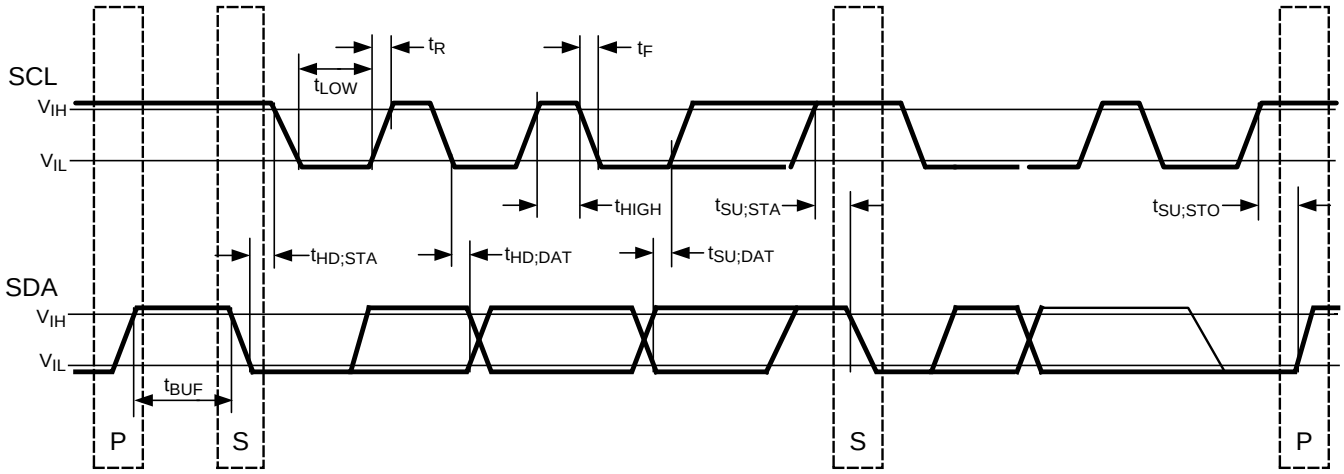


Figure 1. SMBus Timing Diagram

7.8 Typical Characteristics

Unless otherwise specified, the following conditions apply: T_J = 25°C, V_{IN} = 12 V. All graphs show junction temperature.

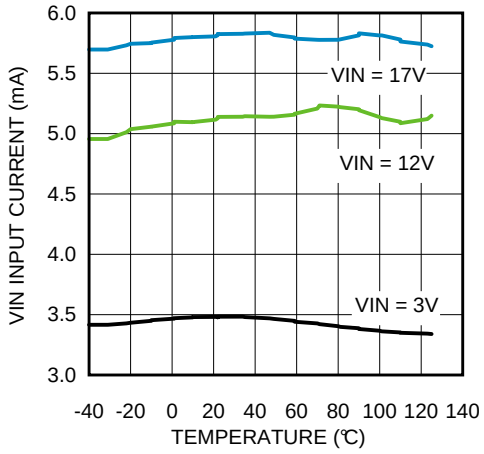


Figure 2. VIN Pin Current

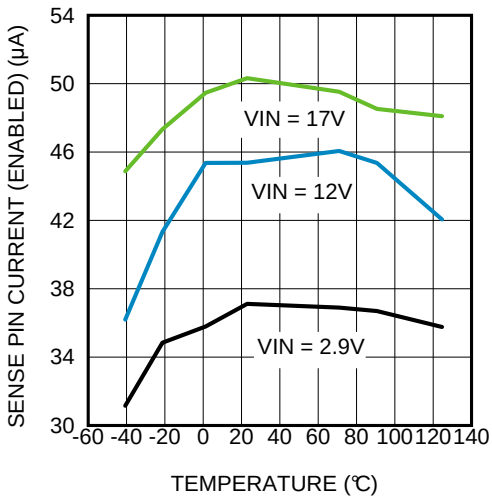


Figure 3. SENSE Pin Current (Enabled)

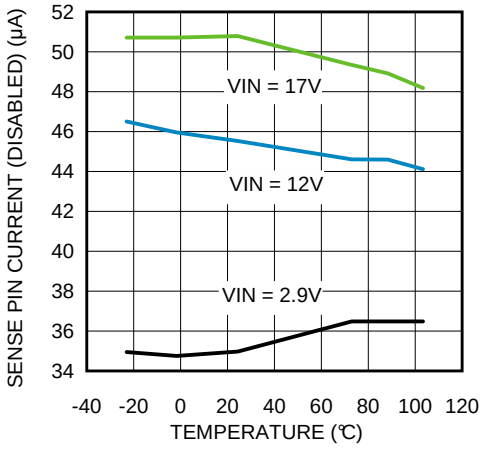


Figure 4. SENSE Pin Current (Disabled)

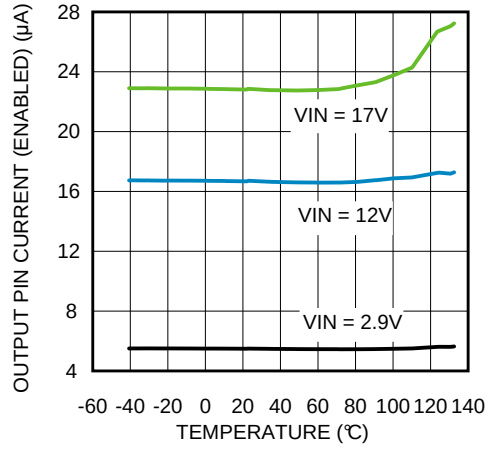


Figure 5. OUT Pin Current (Enabled)

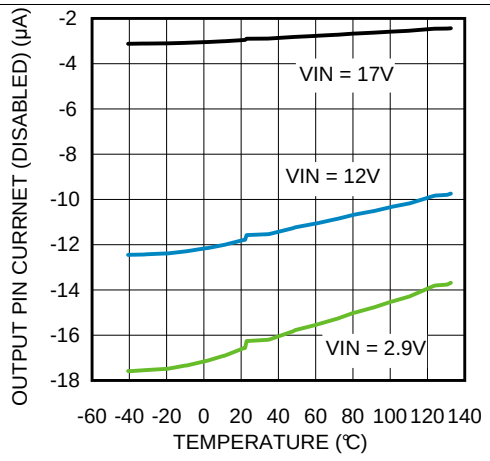


Figure 6. OUT Pin Current (Disabled)

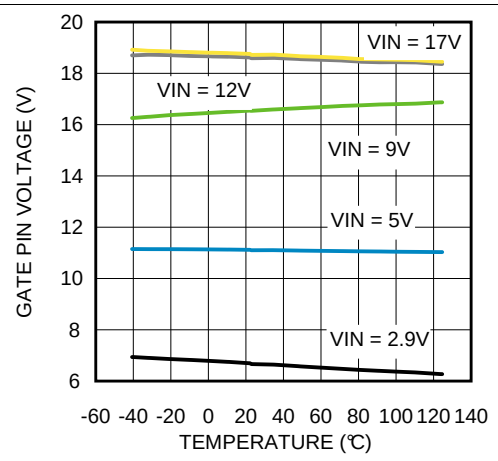


Figure 7. GATE Pin Voltage

Typical Characteristics (continued)

Unless otherwise specified, the following conditions apply: T_J = 25°C, V_{IN} = 12 V. All graphs show junction temperature.

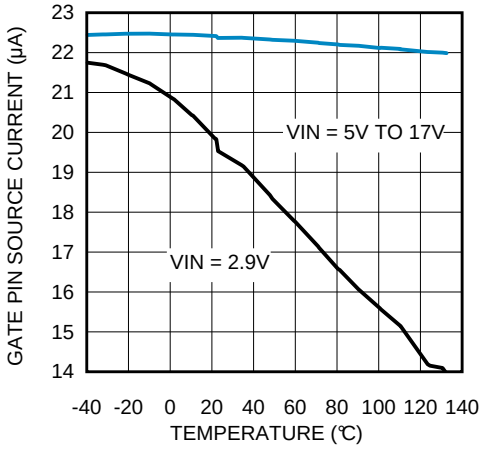


Figure 8. GATE Pin Source Current

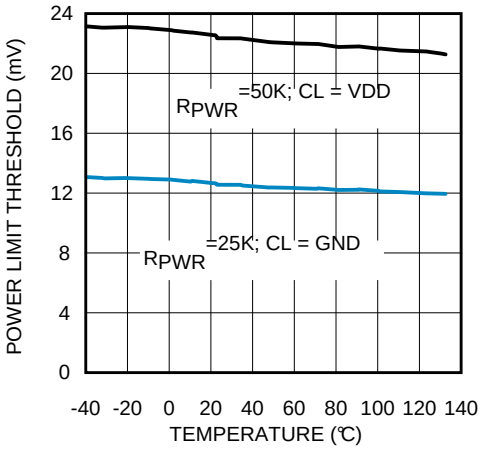


Figure 9. Power Limit Threshold

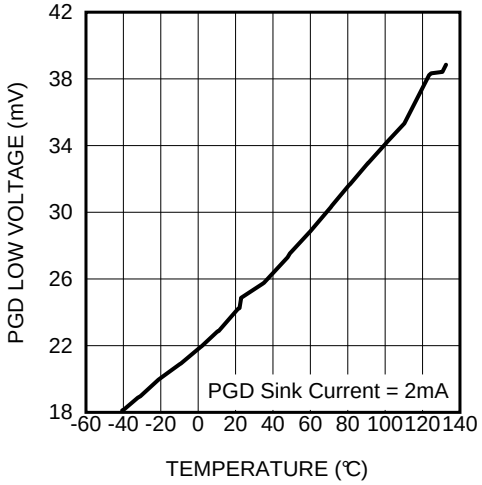


Figure 10. PGD Low Voltage

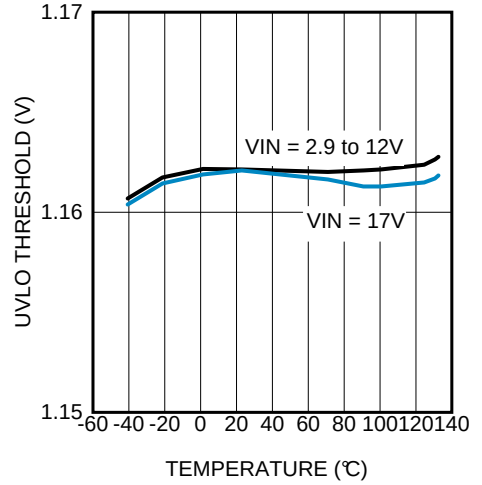


Figure 11. UVLO Threshold

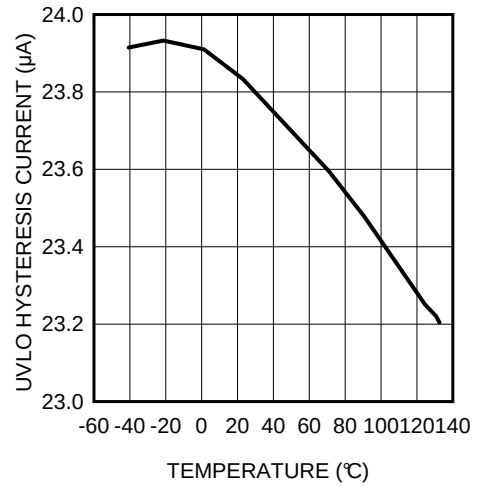


Figure 12. UVLO Hysteresis Current

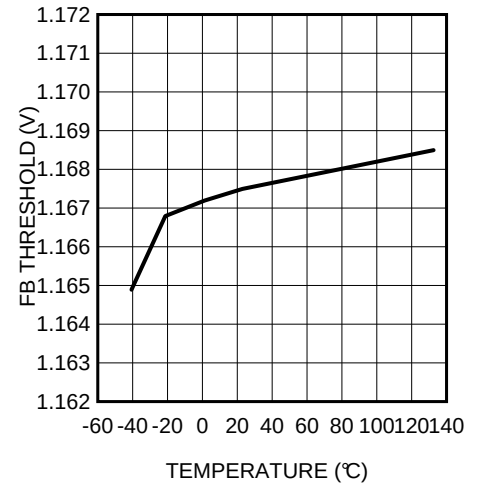


Figure 13. FB Threshold

Typical Characteristics (continued)

Unless otherwise specified, the following conditions apply: T_J = 25°C, V_{IN} = 12 V. All graphs show junction temperature.

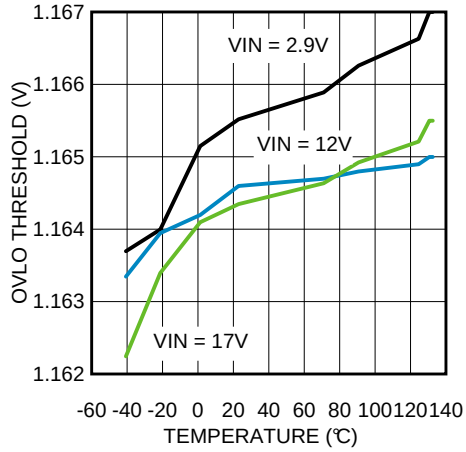


Figure 14. OVLO Threshold

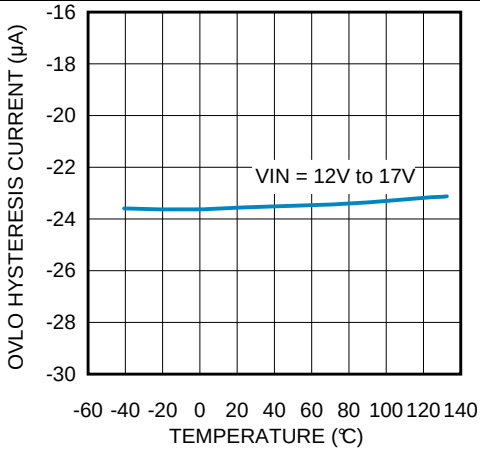


Figure 15. OVLO Hysteresis

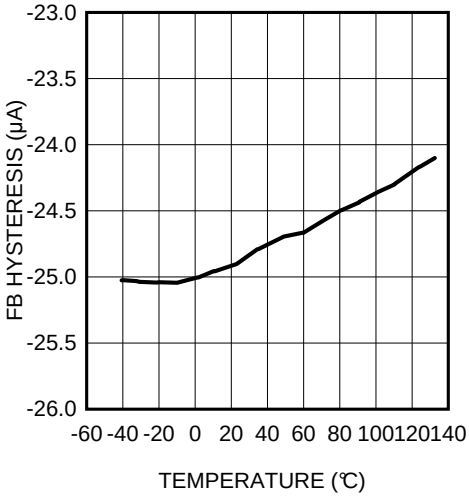


Figure 16. FB Pin Hysteresis

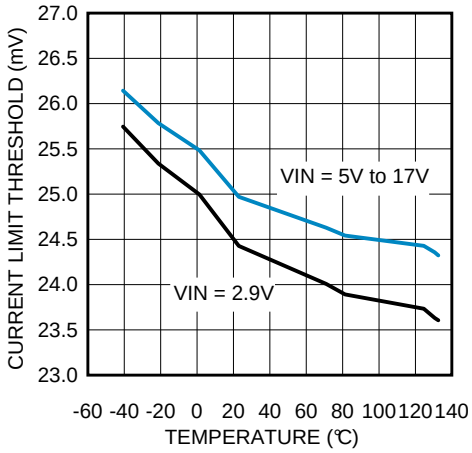


Figure 17. Current Limit Threshold

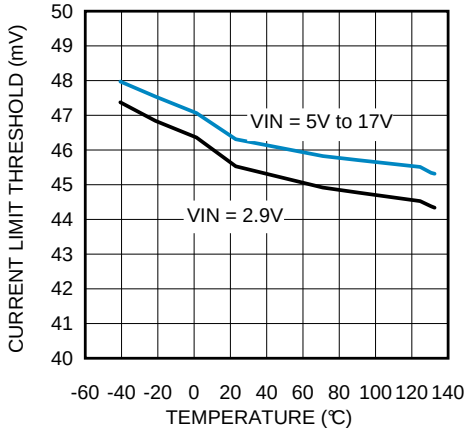


Figure 18. Current Limit Threshold

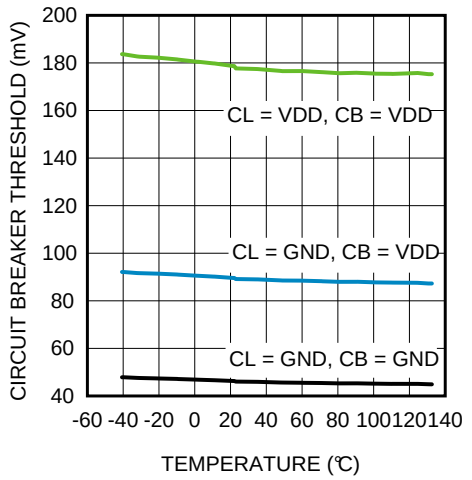


Figure 19. Circuit Breaker Threshold (CL = VDD)

Typical Characteristics (continued)

Unless otherwise specified, the following conditions apply: T_J = 25°C, V_{IN} = 12 V. All graphs show junction temperature.

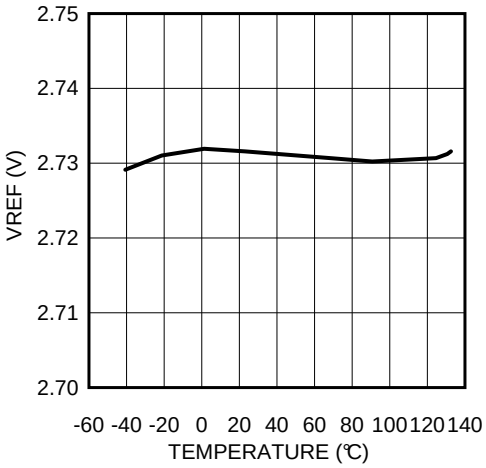


Figure 20. Reference Voltage

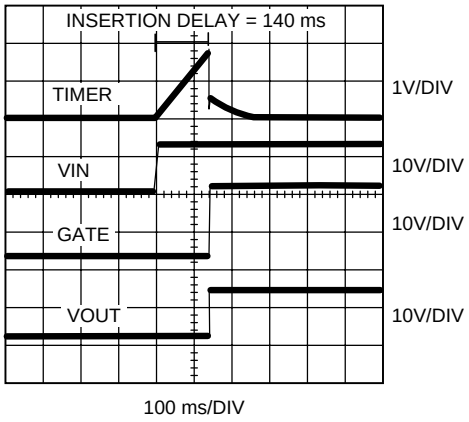


Figure 21. Start-up (Insertion Delay)

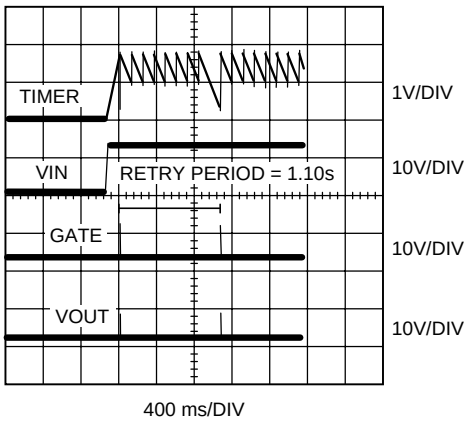


Figure 22. Start-up (Short Circuit V_{OUT})

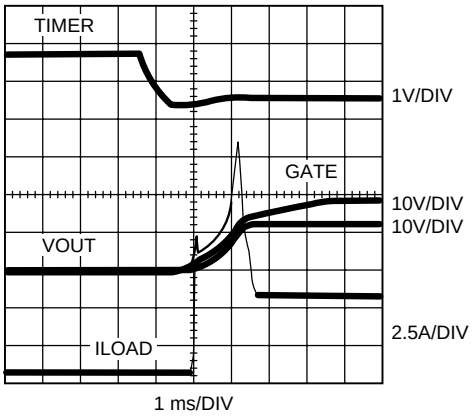


Figure 23. Start-up (5-A Load)

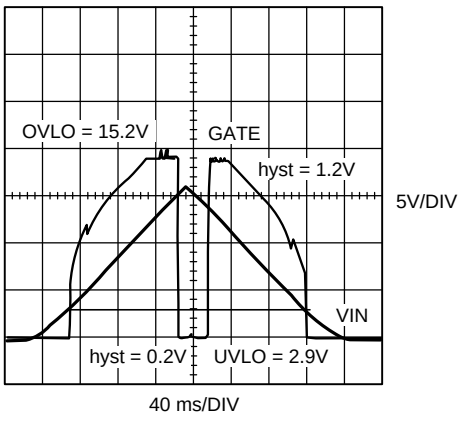


Figure 24. Start-up (UVLO, OVLO)

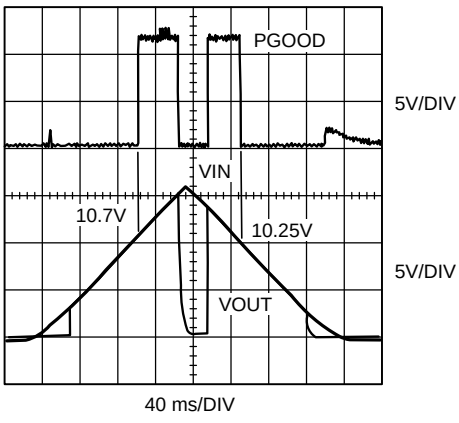


Figure 25. Start-up (PGOOD)

Typical Characteristics (continued)

Unless otherwise specified, the following conditions apply: T_J = 25°C, V_{IN} = 12 V. All graphs show junction temperature.

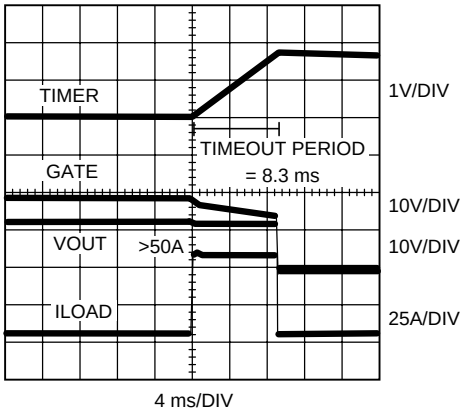


Figure 26. Current Limit Event (CL = GND)

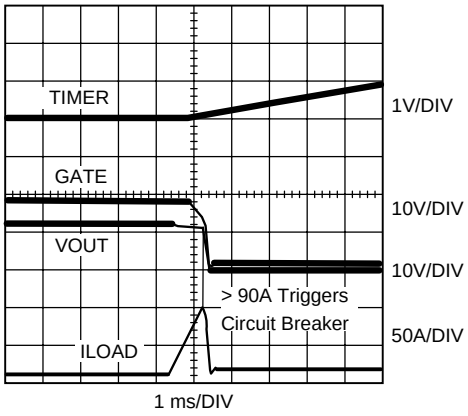


Figure 27. Circuit Breaker Event (CL = CB = GND)

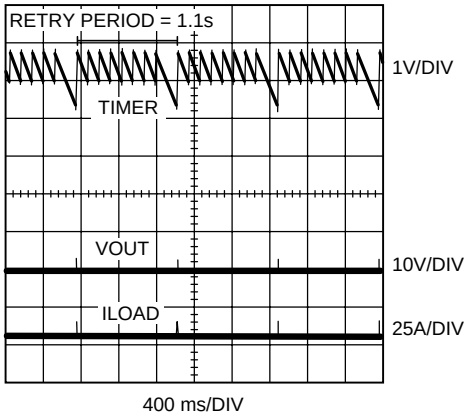


Figure 28. Retry Event (Retry = GND)

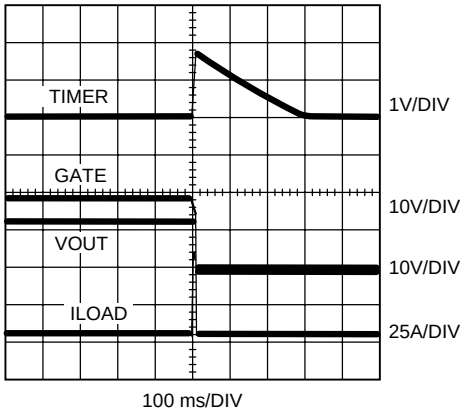


Figure 29. Latch Off (Retry = VDD)

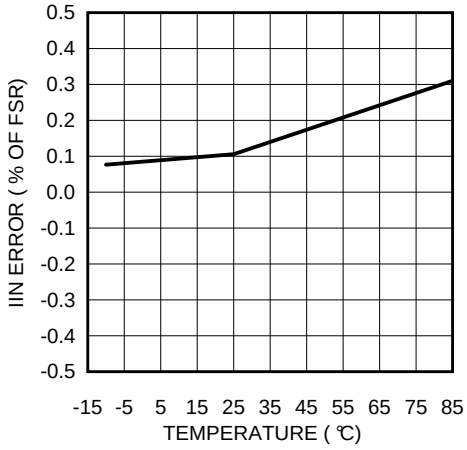


Figure 30. IIN Measurement Accuracy (VIN – SENSE = 25 mV)

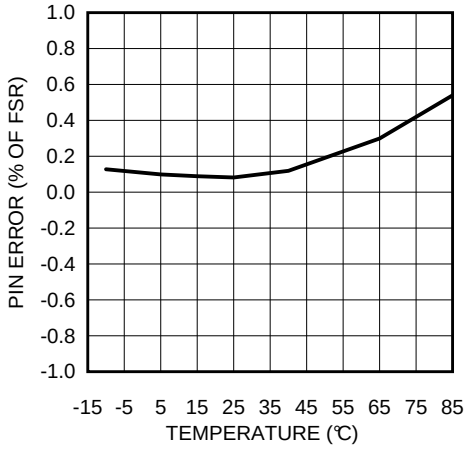


Figure 31. PIN Measurement Accuracy (VIN – SENSE = 25 mV)

8 Detailed Description

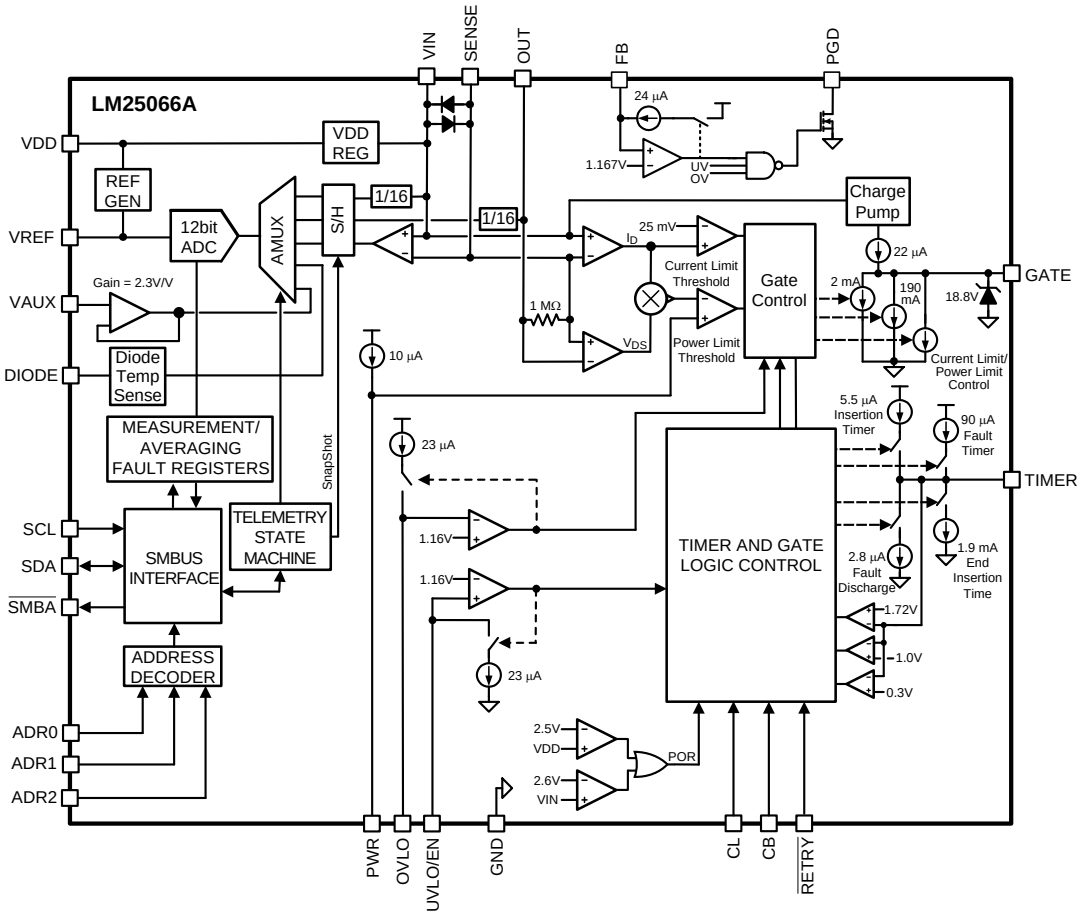
8.1 Overview

The inline protection functionality of the LM25066A is designed to control the in-rush current to the load upon insertion of a circuit card into a live backplane or other *hot* power source, thereby limiting the voltage sag on the backplane's supply voltage and the dV/dt of the voltage applied to the load. Effects on other circuits in the system are minimized, preventing possible unintended resets. A controlled shutdown when the circuit card is removed can also be implemented using the LM25066A.

In addition to a programmable current limit, the LM25066A monitors and limits the maximum power dissipation in the series pass device to maintain operation within the device Safe Operating Area (SOA). Either current limiting or power limiting for an extended period of time results in the shutdown of the series pass device. In this event, the LM25066A can latch off or repetitively retry based on the hardware setting of the $\overline{\text{RETRY}}$ pin. Once started, the number of retries can be set to none, 1, 2, 4, 8, 16, or infinite. The circuit breaker function quickly switches off the series pass device upon detection of a severe overcurrent condition. Programmable undervoltage lockout (UVLO) and overvoltage lockout (OVLO) circuits shut down the LM25066A when the system input voltage is outside the desired operating range.

The telemetry capability of the LM25066A provides intelligent monitoring of the input voltage, output voltage, input current, input power, temperature, and an auxiliary input. The LM25066A also provides a peak capture of the input power and programmable hardware averaging of the input voltage, current, power, and output voltage. Warning thresholds which trigger the $\overline{\text{SMBA}}$ pin may be programmed for input and output voltage, current, power and temperature via the PMBus interface. Additionally, the LM25066A is capable of detecting damage to the external MOSFET, Q_1.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Current Limit

The current limit threshold is reached when the voltage across the sense resistor R_S (VIN to SENSE) exceeds the internal voltage limit of 25 mV or 46 mV depending on whether the CL pin is connected to GND or VDD, respectively. In the current limiting condition, the GATE voltage is controlled to limit the current in MOSFET Q_1. While the current limit circuit is active, the fault timer is active as described in *Fault Timer and Restart*. If the load current falls below the current limit threshold before the end of the Fault Timeout Period, the LM25066A resumes normal operation. If the current limit condition persists for longer than the Fault Timeout Period set by the timer capacitor, C_T, the IIN OC FAULT bit in the *MFR_SPECIFIC_17: READ_DIAGNOSTIC_WORD (E1h)* register, the INPUT bit in the *STATUS_WORD (79h)* register, and the IIN_OC/PFET_OP_FAULT bit in the register will be toggled high and SMBA pin will be pulled low unless this feature is disabled using the *MFR_SPECIFIC_08: ALERT_MASK (D8h)* register. For proper operation, the R_S resistor value should be less than 200 mΩ. Higher values may create instability in the current limit control loop. The current limit threshold pin value may be overridden by setting appropriate bits in the *MFR_SPECIFIC_09: DEVICE_SETUP (D9h)*.

8.3.2 Circuit Breaker

If the load current increases rapidly (for example, the load is short-circuited), the current in the sense resistor (R_S) may exceed the current limit threshold before the current limit control loop is able to respond. If the current exceeds 1.8 or 3.6 times (user settable) the current limit threshold, Q_1 is quickly switched off by the 190-mA pulldown current at the GATE pin, and a Fault Timeout Period begins. When the voltage across R_S falls below the threshold the 190-mA pulldown current at the GATE pin is switched off and the gate voltage of Q_1 is then

Feature Description (continued)

determined by the current limit or power limit functions. If the TIMER pin reaches 1.7 V before the current limiting or power limiting condition ceases, Q_1 is switched off by the 2-mA pulldown current at the GATE pin as described in *Fault Timer and Restart*. A circuit breaker event will cause the CIRCUIT BREAKER FAULT bit in the *STATUS_MFR_SPECIFIC (80h)* and *MFR_SPECIFIC_17: READ_DIAGNOSTIC_WORD (E1h)* registers to be toggled high and $\overline{\text{SMBA}}$ pin will be pulled low unless this feature is disabled using the *MFR_SPECIFIC_08: ALERT_MASK (D8h)* register. The circuit breaker pin configuration may be overridden by setting appropriate bits in the *MFR_SPECIFIC_09: DEVICE_SETUP (D9h)*) register.

8.3.3 Power Limit

An important feature of the LM25066A is the MOSFET power limiting. The Power Limit function can be used to maintain the maximum power dissipation of MOSFET Q_1 within the device SOA rating. The LM25066A determines the power dissipation in Q_1 by monitoring its drain-source voltage (SENSE to OUT), and the drain current through R_S (VIN to SENSE). The product of the current and voltage is compared to the power limit threshold programmed by the resistor at the PWR pin. If the power dissipation reaches the limiting threshold, the GATE voltage is controlled to regulate the current in Q_1. While the power limiting circuit is active, the fault timer is active as described in *Fault Timer and Restart*. If the power limit condition persists for longer than the Fault Timeout Period set by the timer capacitor, C_T, the IIN_OC_FAULT bit in the *STATUS_INPUT (7Ch)* register, the INPUT bit in the *STATUS_WORD (79h)* register, and the IIN_OC/PFET_OP_$\overline{\text{FAULT}}$ bit in the*MFR_SPECIFIC_17: READ_DIAGNOSTIC_WORD (E1h)* register will be toggled high and $\overline{\text{SMBA}}$ pin will be pulled low unless this feature is disabled using the *MFR_SPECIFIC_08: ALERT_MASK (D8h)* register.

8.3.4 Undervoltage Lockout (UVLO)

The series pass MOSFET (Q_1) is enabled when the input supply voltage (V_{SYS}) is within the operating range defined by the programmable undervoltage lockout (UVLO) and overvoltage lockout (OVLO) levels. Typically the UVLO level at V_{SYS} is set with a resistor divider (R1-R3) as shown in Figure 35. Refering to the Block Diagram when V_{SYS} is below the UVLO level, the internal 23-µA current source at UVLO is enabled, the current source at OVLO is off, and Q_1 is held off by the 2-mA pulldown current at the GATE pin. As V_{SYS} is increased, raising the voltage at UVLO above its threshold the 23-µA current source at UVLO is switched off, increasing the voltage at UVLO, providing hysteresis for this threshold. With the UVLO/EN pin above its threshold, Q_1 is switched on by the 22-µA current source at the GATE pin if the insertion time delay has expired.

See *Typical Application* for a procedure to calculate the values of the threshold setting resistors (R1-R3). The minimum possible UVLO level at V_{SYS} can be set by connecting the UVLO/EN pin to VIN. In this case, Q_1 is enabled after the insertion time when the voltage at VIN reaches the POR threshold. After power up, an UVLO condition will toggle high the VIN UV FAULT bit in the *STATUS_INPUT (7Ch)*, the INPUT bit in the *STATUS_WORD (79h)* register, and the VIN_$\overline{\text{UNDER}}$VOLTAGE_FAULT bit in the *MFR_SPECIFIC_17: READ_DIAGNOSTIC_WORD (E1h)* register, and $\overline{\text{SMBA}}$ pin will be pulled low unless this feature is disabled using the *MFR_SPECIFIC_08: ALERT_MASK (D8h)* register.

8.3.5 Overvoltage Lockout (OVLO)

The series pass MOSFET (Q_1) is enabled when the input supply voltage (V_{SYS}) is within the operating range defined by the programmable undervoltage lockout (UVLO) and overvoltage lockout (OVLO) levels. If V_{SYS} raises the OVLO pin voltage above its threshold, Q_1 is switched off by the 2-mA pulldown current at the GATE pin, denying power to the load. When the OVLO pin is above its threshold, the internal 23 µA current source at OVLO is switched on, raising the voltage at OVLO to provide threshold hysteresis. When V_{SYS} is reduced below the OVLO level, Q_1 is re-enabled. An OVLO condition will toggle high the VIN OV FAULT bit in the *STATUS_INPUT (7Ch)*, the INPUT bit in the *STATUS_WORD (79h)* register, and the VIN_$\overline{\text{OVER}}$VOLTAGE_FAULT bit in the *MFR_SPECIFIC_17: READ_DIAGNOSTIC_WORD (E1h)* register, and the $\overline{\text{SMBA}}$ pin will be pulled low unless this feature is disabled using the *MFR_SPECIFIC_08: ALERT_MASK (D8h)* register.

See *Typical Application* for a procedure to calculate the threshold setting resistor values.

Feature Description (continued)

8.3.6 Power Good

The Power Good indicator (PGD) is connected to the drain of an internal N-channel MOSFET capable of sustaining 17 V in the off-state, and transients up to 20 V. An external pullup resistor is required at PGD to an appropriate voltage to indicate the status to downstream circuitry. The off-state voltage at the PGD pin can be higher or lower than the voltages at VIN and OUT. PGD is switched high when the voltage at the FB pin exceeds the PGD threshold voltage. Typically, the output voltage threshold is set with a resistor divider from output to feedback, although the monitored voltage need not be the output voltage. Any other voltage can be monitored as long as the voltage at the FB pin does not exceed its maximum rating. Referring to the Block Diagram, when the voltage at the FB pin is below its threshold, the 24-µA current source at FB is disabled. As the output voltage increases, taking FB above its threshold, the current source is enabled, sourcing current out of the pin, raising the voltage at FB to provide threshold hysteresis. The PGD output is forced low when either the UVLO/EN pin is below its threshold or the OVLO pin is above its threshold. The status of the PGD pin can be read via the PMBus interface in either the *STATUS_WORD (79h)* or *MFR_SPECIFIC_17: READ_DIAGNOSTIC_WORD (E1h)* registers.

8.3.7 VDD Sub-Regulator

The LM25066A contains an internal linear sub-regulator which steps down the input voltage to generate a 4.5 V rail used for powering low voltage circuitry. When the input voltage is below 4.5 V, VDD will track VIN. For input voltages 3.3 V and below, VDD should be tied directly to VIN to avoid the dropout of the sub-regulator. The VDD sub-regulator should be used as the pullup supply for the CL, CB, $\overline{\text{RETRY}}$, ADR2, ADR1, ADR0 pins if they are to be tied high. It may also be used as the pullup supply for the PGD and the SMBus signals (SDA, SCL, $\overline{\text{SMBA}}$). The VDD sub-regulator is not designed to drive high currents and should not be loaded with other integrated circuits. The VDD pin is current limited to 45 mA in order to protect the LM25066A in the event of a short. The sub-regulator requires a bypass capacitance having a value from 1 µF to 4.7 µF to be placed as close to the VDD pin as the PCB layout allows.

Feature Description (continued)

8.3.8 Remote Temperature Sensing

The LM25066A is designed to measure temperature remotely using an MMBT3904 NPN transistor. The base and collector of the MMBT3904 is connected to the DIODE pin and the emitter is grounded. Place the MMBT3904 near the device whose temperature is to be monitored. If the temperature of the hot-swap pass MOSFET, Q_1, is to be measured, the MMBT3904 should be placed as close to Q_1 as the layout allows. The temperature is measured by means of a change in the diode voltage in response to a step in current supplied by the DIODE pin. The DIODE pin sources a constant 9.4 µA but pulses 250 µA once every millisecond in order to measure the diode temperature. Care must be taken in the PCB layout to keep the parasitic resistance between the DIODE pin and the MMBT3904 low so as not to degrade the measurement. Additionally, a small 1000-pF bypass capacitor should be placed in parallel with the MMBT3904 to reduce the effects of noise. The temperature can be read using the *READ_TEMPERATURE_1 (8Dh)* PMBus command. The default limits of the LM25066A will cause $\overline{\text{SMBA}}$ pin to be pulled low if the measured temperature exceeds 125°C and will disable the hot-swap pass MOSFET if the temperature exceeds 150°C. These thresholds can be reprogrammed via the PMBus interface using the *OT_WARN_LIMIT (51h)* and *OT_FAULT_LIMIT (4Fh)* commands. If the temperature measurement and protection capability of the LM25066A is not used, the DIODE pin should be grounded.

8.3.9 Damaged MOSFET Detection

The LM25066A is able to detect whether the external MOSFET, Q_1, is damaged under certain conditions. If the voltage across the sense resistor exceeds 4 mV while the GATE voltage is low or the internal logic indicates that the GATE should be low, the EXT_MOSFET_SHORTED bit in the *STATUS_MFR_SPECIFIC (80h)* and *MFR_SPECIFIC_17: READ_DIAGNOSTIC_WORD (E1h)* registers will be toggled high and the $\overline{\text{SMBA}}$ pin will be pulled low unless this feature is disabled using the *MFR_SPECIFIC_08: ALERT_MASK (D8h)*. This method effectively determines whether Q_1 is shorted because of damage present between the drain and gate and/or drain and source of the external MOSFET.

8.4 Device Functional Modes

8.4.1 Power Up Sequence

The VIN operating range of the LM25066A is +2.9 V to +17 V, with transient capability to +24 V. Referring to Figure 38 and Figure 32, as the voltage at VIN initially increases, the external N-channel MOSFET (Q_1) is held off by an internal 190-mA pulldown current at the GATE pin. The strong pulldown current at the GATE pin prevents an inadvertent turnon as the MOSFET's gate-to-drain (Miller) capacitance is charged. Additionally, the TIMER pin is initially held at ground. When the V_{IN} voltage reaches the POR threshold, the insertion time begins. During the insertion time, the capacitor at the TIMER pin (C_T) is charged by a 5.5-µA current source and Q_1 is held off by a 2-mA pulldown current at the GATE pin regardless of the input voltage. The insertion time delay allows ringing and transients at VIN to settle before Q_1 is enabled. The insertion time ends when the TIMER pin voltage reaches 1.7 V. C_T is then quickly discharged by an internal 1.9-mA pulldown current. The GATE pin then switches on Q_1 when V_{SYS}, the input supply voltage, exceeds the UVLO threshold. If V_{SYS} is above the UVLO threshold at the end of the insertion time, Q_1 switches on at that time. The GATE pin charge pump sources 22 µA to charge the gate capacitance of Q_1. The maximum voltage at the GATE pin with respect to ground is limited by an internal 18.8-V Zener diode.

As the voltage at the OUT pin increases, the LM25066A monitors the drain current and power dissipation of MOSFET Q_1. Inrush current limiting and/or power limiting circuits actively control the current delivered to the load. During the inrush limiting interval (t_2 in Figure 32), an internal 90-A fault timer current source charges C_T. If Q_1's power dissipation and the input current reduce below their respective limiting thresholds before the TIMER pin reaches 1.7 V, the 90-µA current source is switched off and C_T is discharged by the internal 2.8-µA current sink (t_3 in Figure 32). The PGD pin switches high when FB exceeds its rising threshold of 1.167 V.

If the TIMER pin voltage reaches 1.7 V before inrush current limiting or power limiting ceases during t_2, a fault is declared and Q_1 is turned off. See *Fault Timer and Restart* for a complete description of the fault mode.

The LM25066A will pull the $\overline{\text{SMBA}}$ pin low after the input voltage has exceeded its POR threshold to indicate that the volatile memory and device settings are in their default state. The CONFIG_PRESET bit within the *STATUS_MFR_SPECIFIC (80h)* indicates default configuration of warning thresholds and device operation and will remain set until a CLEAR_FAULTS command is received.

Device Functional Modes (continued)

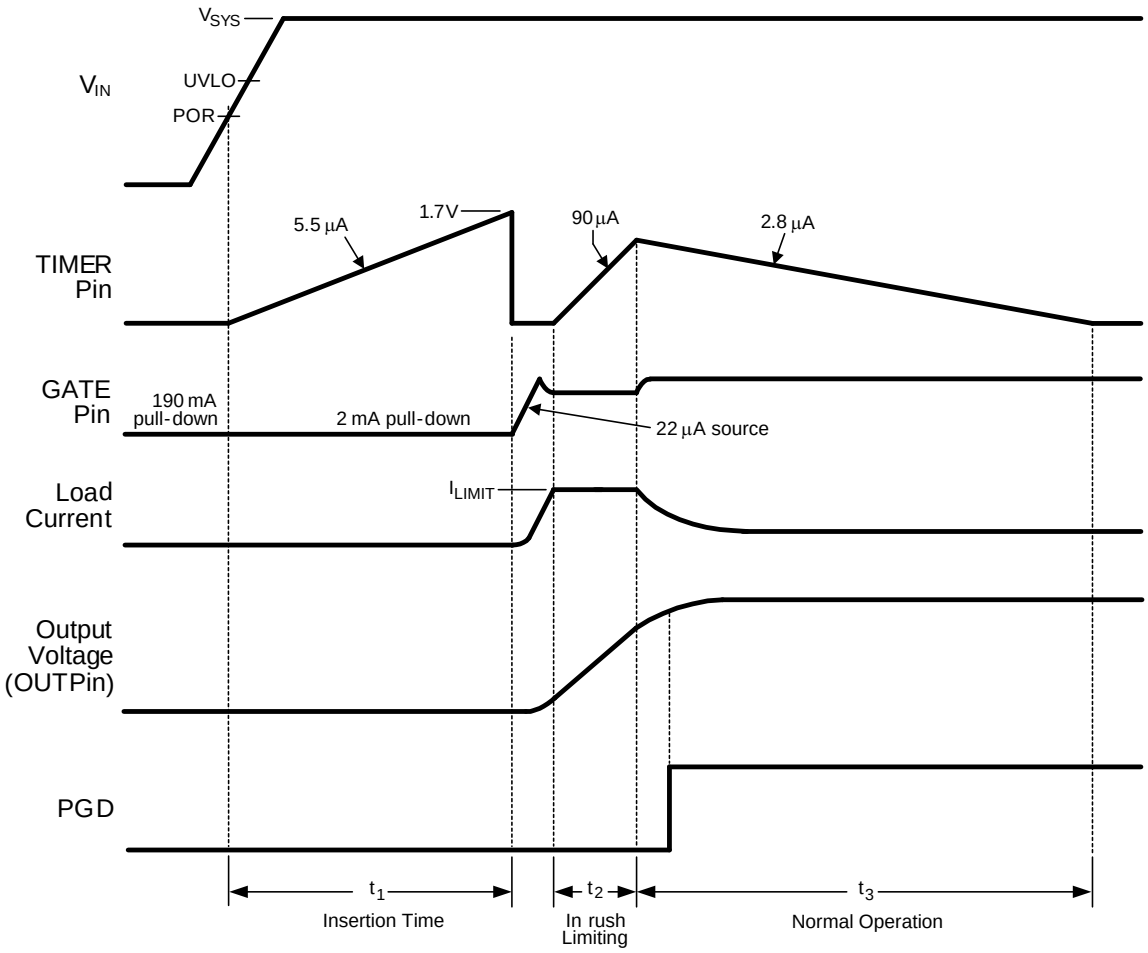


Figure 32. Power Up Sequence (Current Limit Only)

8.4.2 Gate Control

A charge pump provides the voltage at the GATE pin to enhance the N-Channel MOSFET's gate. During normal operating conditions (t_3 in Figure 32) the gate of Q_1 is held charged by an internal 22-µA current source. The voltage at the GATE pin (with respect to ground) is limited by an internal 18.8-V Zener diode. See Figure 7. Since the gate-to-source voltage applied to Q_1 could be as high as 18.8 V during various conditions, a Zener diode with the appropriate voltage rating must be added between the GATE and OUT pins if the maximum V_{GS} rating of the selected MOSFET is less than 18.8 V. The external Zener diode must have a forward current rating of at least 190 mA. When the system voltage is initially applied, the GATE pin is held low by a 190-mA pulldown current. This helps prevent an inadvertent turnon of the MOSFET through its drain-gate capacitance as the applied system voltage increases.

During the insertion time (t_1 in Figure 32) the GATE pin is held low by a 2-mA pulldown current. This maintains Q_1 in the off-state until the end of t_1, regardless of the voltage at VIN or UVLO. Following the insertion time (t_2 in Figure 32), the gate voltage of Q_1 is controlled to keep the current or power dissipation level from exceeding the programmed levels. While in the current or power limiting mode, the TIMER pin capacitor is charging. If the current and power limiting cease before the TIMER pin reaches 1.7 V, the TIMER pin capacitor then discharges, and the circuit begins normal operation. If the inrush limiting condition persists such that the TIMER pin reached 1.7 V during t_2, the GATE pin is then pulled low by the 190-mA pulldown current. The GATE pin is then held low until either a power up sequence is initiated ($\overline{\text{RETRY}}$ pin to VDD), or an automatic retry is attempted ($\overline{\text{RETRY}}$ pin to GROUND). See *Fault Timer and Restart*. If the system input voltage falls below the UVLO threshold or rises above the OVLO threshold, the GATE pin is pulled low by the 2-mA pulldown current to switch off Q_1.

Device Functional Modes (continued)

8.4.3 Fault Timer and Restart

When the current limit or power limit threshold is reached during turnon, or as a result of a fault condition, the gate-to-source voltage of Q_1 is controlled to regulate the load current and power dissipation in Q_1. When either limiting function is active, a 90-µA fault timer current source charges the external capacitor (C_T) at the TIMER pin as shown in Figure 32 (Fault Timeout Period). If the fault condition subsides during the Fault Timeout Period before the TIMER pin reaches 1.7 V, the LM25066A returns to the normal operating mode and C_T is discharged by the 1.9-mA current sink. If the TIMER pin reaches 1.7 V during the Fault Timeout Period, Q_1 is switched off by a 2-mA pulldown current at the GATE pin. The subsequent restart procedure then depends on the selected retry configuration.

If the $\overline{\text{RETRY}}$ pin is high, the LM25066A latches the GATE pin low at the end of the Fault Timeout Period. C_T is then discharged to ground by the 2.8-µA fault current sink. The GATE pin is held low by the 2-mA pulldown current until a power up sequence is externally initiated by cycling the input voltage (V_{SYS}), or momentarily pulling the UVLO/EN pin below its threshold with an open-collector or open-drain device as shown in Figure 33. The voltage at the TIMER pin must be <0.3 V for the restart procedure to be effective. The TIMER_LATCHED_OFF bit in the *MFR_SPECIFIC_17: READ_DIAGNOSTIC_WORD (E1h)* register will remain high while the latched off condition persists.

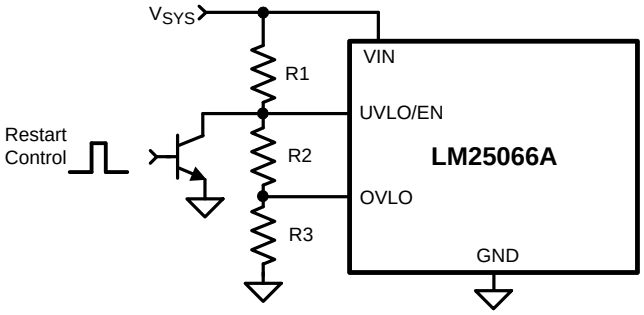


Figure 33. Latched Fault Restart Control

The LM25066A provides an automatic restart sequence which consists of the TIMER pin cycling between 1.7 V and 1 V seven times after the Fault Timeout Period, as shown in Figure 34. The period of each cycle is determined by the 90-µA charging current, and the 2.8-µA discharge current, and the value of the capacitor C_T. When the TIMER pin reaches 0.3 V during the eighth high-to-low ramp, the 22-µA current source at the GATE pin turns on Q_1. If the fault condition is still present, the Fault Timeout Period and the restart sequence repeat. The $\overline{\text{RETRY}}$ pin allows selecting no retries or infinite retries. Finer control of the retry behavior can be achieved through the *MFR_SPECIFIC_09: DEVICE_SETUP (D9h)* register. Retry counts of 0, 1, 2, 4, 8, 16 or infinite may be selected by setting the appropriate bits in the *MFR_SPECIFIC_09: DEVICE_SETUP (D9h)* register.

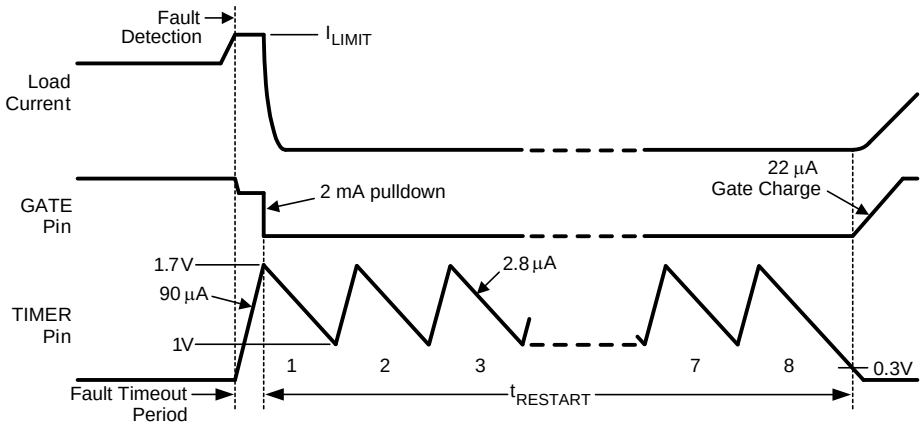


Figure 34. Restart Sequence

Device Functional Modes (continued)

8.4.4 Shutdown Control

The load current can be remotely switched off by taking the UVLO/EN pin below its threshold with an open collector or open drain device, as shown in Figure 35. Upon releasing the UVLO/EN pin, the LM25066A switches on the load current with inrush current and power limiting.

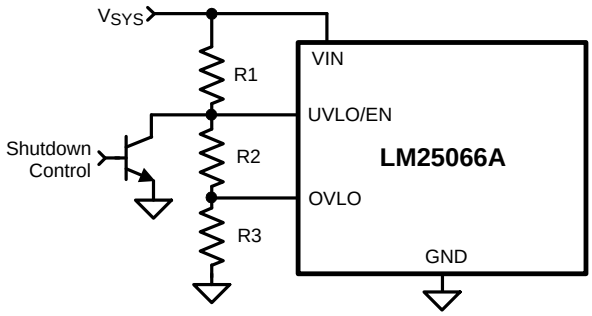


Figure 35. Shutdown Control

8.4.5 Enabling/Disabling and Resetting

The output can be disabled at any time during normal operation by either pulling the UVLO/EN pin to below its threshold or the OVLO pin above its threshold, causing the GATE voltage to be forced low with a pulldown strength of 2 mA. Toggling the UVLO/EN pin will also reset the LM25066A from a latched-off state due to an overcurrent or over-power limit condition which has caused the maximum allowed number of retries to be exceeded. While the UVLO/EN or OVLO pins can be used to disable the output, they have no effect on the volatile memory or address location of the LM25066A. User stored values for address, device operation, and warning and fault levels programmed via the SMBus are preserved while the LM25066A is powered regardless of the state of the UVLO/EN and OVLO pins. The output may also be enabled or disabled by writing 80h or 0h to the OPERATION (03h) register. To re-enable after a fault, the fault condition should be cleared and the OPERATION (03h) register should be written to 0h and then 80h.

The SMBus address of the LM25066A is captured based on the states of the ADR0, ADR1, and ADR2 pins (GND, NC, VDD) during turnon and is latched into a volatile register once VDD has exceeded its POR threshold of 2.6 V. Reassigning or postponing the address capture is accomplished by holding the VREF pin to ground. Pulling the VREF pin low will also reset the logic and erase the volatile memory of the LM25066A. Once released, the VREF pin will charge up to its final value and the address will be latched into a volatile register once the voltage at the VREF exceeds 2.4 V.

8.5 Register Maps

8.5.1 PMBus Command Support

The device features an SMBus interface that allows the use of PMBus™ commands to set warn levels, error masks, and get telemetry on V_{IN}, V_{OUT}, I_{IN}, V_{AUX}, and P_{IN}. The supported PMBus™ commands are shown in Table 1.

Table 1. Supported PMBus™ Commands

CODE	NAME	FUNCTION	R/W	NUMBER OF DATA BYTES	DEFAULT VALUE
01h	OPERATION	Retrieves or stores the operation status	R/W	1	80h
03h	CLEAR_FAULTS	Clears the status registers and re-arms the black box registers for updating	Send Byte	0	
19h	CAPABILITY	Retrieves the device capability	R	1	B0h
43h	VOUT_UV_WARN_LIMIT	Retrieves or stores output undervoltage warn limit threshold	R/W	2	0000h
4Fh	OT_FAULT_LIMIT	Retrieves or stores over-temperature fault limit threshold	R/W	2	0960h (150°C)
51h	OT_WARN_LIMIT	Retrieves or stores over-temperature warn limit threshold	R/W	2	07D0h (125°C)
57h	VIN_OV_WARN_LIMIT	Retrieves or stores input overvoltage warn limit threshold	R/W	2	0FFFh
58h	VIN_UV_WARN_LIMIT	Retrieves or stores input undervoltage warn limit threshold	R/W	2	0000h
78h	STATUS_BYTE	Retrieves information about the part operating status	R	1	49h
79h	STATUS_WORD	Retrieves information about the part operating status	R	2	3849h
7Ah	STATUS_VOUT	Retrieves information about output voltage status	R	1	00h
7Ch	STATUS_INPUT	Retrieves information about input status	R	1	10h
7Dh	STATUS_TEMPERATURE	Retrieves information about temperature status	R	1	00h
7Eh	STATUS_CML	Retrieves information about communications status	R	1	00h
80h	STATUS_MFR_SPECIFIC	Retrieves information about circuit breaker and MOSFET shorted status	R	1	10h
88h	READ_VIN	Retrieves input voltage measurement	R	2	0000h
8Bh	READ_VOUT	Retrieves output voltage measurement	R	2	0000h
8Dh	READ_TEMPERATURE_1	Retrieves temperature measurement	R	2	0190h
99h	MFR_ID	Retrieves manufacturer ID in ASCII characters (NSC)	R	3	4Eh 53h 43h
9Ah	MFR_MODEL	Retrieves part number in ASCII characters (LM25066A)	R	8	4Ch 4Dh 32h 35h 30h 36h 36h 0h
9Bh	MFR_REVISION	Retrieves part revision letter or number in ASCII (for example, AA)	R	2	41h 41h
D0h	MFR_SPECIFIC_00 READ_VAUX	Retrieves auxiliary voltage measurement	R	2	0000h
D1h	MFR_SPECIFIC_01 MFR_READ_IIN	Retrieves input current measurement	R	2	0000h
D2h	MFR_SPECIFIC_02 MFR_READ_PIN	Retrieves input power measurement	R	2	0000h
D3h	MFR_SPECIFIC_03 MFR_IIN_OC_WARN_LIMIT	Retrieves or stores input current limit warn threshold	R/W	2	0FFFh

Register Maps (continued)

Table 1. Supported PMBus™ Commands (continued)

CODE	NAME	FUNCTION	R/W	NUMBER OF DATA BYTES	DEFAULT VALUE
D4h	MFR_SPECIFIC_04 MFR_PIN_OP_WARN_LIMIT	Retrieves or stores input power limit warn threshold	R/W	2	0FFFh
D5h	MFR_SPECIFIC_05 READ_PIN_PEAK	Retrieves measured maximum input power measurement	R	2	0000h
D6h	MFR_SPECIFIC_06 CLEAR_PIN_PEAK	Resets the contents of the peak input power register to zero	Send Byte	0	
D7h	MFR_SPECIFIC_07 GATE_MASK	Disables external MOSFET gate control for FAULTs	R/W	1	0000h
D8h	MFR_SPECIFIC_08 ALERT_MASK	Retrieves or stores user $\overline{\text{SMBA}}$ fault mask	R/W	2	0820h
D9h	MFR_SPECIFIC_09 DEVICE_SETUP	Retrieves or stores information about number of retry attempts	R/W	1	0000h
DAh	MFR_SPECIFIC_10 BLOCK_READ	Retrieves most recent diagnostic and telemetry information in a single transaction	R	12	0460h 0000h 0000h 0000h 0000h 0000h
DBh	MFR_SPECIFIC_11 SAMPLES_FOR_AVG	Exponent value AVGN for number of samples to be averaged, range = 00h to 0Ch	R/W	1	00h
DCh	MFR_SPECIFIC_12 READ_AVG_VIN	Retrieves averaged input voltage measurement	R	2	0000h
DDh	MFR_SPECIFIC_13 READ_AVG_VOUT	Retrieves averaged output voltage measurement	R	2	0000h
DEh	MFR_SPECIFIC_14 READ_AVG_IIN	Retrieves averaged input current measurement	R	2	0000h
DFh	MFR_SPECIFIC_15 READ_AVG_PIN	Retrieves averaged input power measurement	R	2	0000h
E0h	MFR_SPECIFIC_16 BLACK_BOX_READ	Captures diagnostic and telemetry information which are latched when the first $\overline{\text{SMBA}}$ alert occurs after faults have been cleared	R	12	0000h 0000h 0000h 0000h 0000h 0000h
E1h	MFR_SPECIFIC_17 READ_DIAGNOSTIC_WORD	Manufacturer-specific parallel of the STATUS_WORD to convey all FAULT/WARN data in a single transaction	R	2	0460h
E2h	MFR_SPECIFIC_18 AVG_BLOCK_READ	Retrieves most recent average telemetry and diagnostic information in a single transaction	R	12	0460h 0000h 0000h 0000h 0000h 0000h

8.5.1.1 Standard PMBus™ Commands

8.5.1.1.1 OPERATION (01h)

The OPERATION command is a standard PMBus™ command that controls the MOSFET switch. This command may be used to switch the MOSFET ON and OFF under host control. It is also used to re-enable the MOSFET after a fault triggered shutdown. Writing an OFF command followed by an ON command will clear all faults. Writing only an ON command after a fault triggered shutdown will not clear the fault registers. The OPERATION command is issued with the write byte protocol.

Table 2. Recognized OPERATION Command Values

VALUE	MEANING	DEFAULT
80h	Switch ON	80h
00h	Switch OFF	–

8.5.1.1.2 CLEAR_FAULTS (03h)

The CLEAR_FAULTS command is a standard PMBus™ command that resets all stored warning and fault flags and the SMBA signal. If a fault or warning condition still exists when the CLEAR_FAULTS command is issued, the SMBA signal may not clear or will re-assert almost immediately. Issuing a CLEAR_FAULTS command will not cause the MOSFET to switch back on in the event of a fault turnoff: that must be done by issuing an OPERATION command after the fault condition is cleared. This command uses the PMBus™ send byte protocol.

8.5.1.1.3 CAPABILITY (19h)

The CAPABILITY command is a standard PMBus™ command that returns information about the PMBus™ functions supported by the LM25066A. This command is read with the PMBus™ read byte protocol.

Table 3. CAPABILITY Register

VALUE	MEANING	DEFAULT
B0h	Supports packet error check, 400 Kbits/sec, supports SMBus alert	B0h

8.5.1.1.4 VOUT_UV_WARN_LIMIT (43h)

The VOUT_UV_WARN_LIMIT command is a standard PMBus™ command that allows configuring or reading the threshold for the VOUT Undervoltage Warning detection. Reading and writing to this register should use the coefficients shown in Table 41. Accesses to this command should use the PMBus™ read or write word protocol. If the measured value of VOUT falls below the value in this register, VOUT UV Warn Limit flags are set in the respective registers, and the SMBA signal is asserted.

Table 4. VOUT_UV_WARN_LIMIT Register

VALUE	MEANING	DEFAULT
1h – 0FFFh	VOUT undervoltage warning detection threshold	0000h (disabled)
0000h	VOUT undervoltage warning disabled	–

8.5.1.1.5 OT_FAULT_LIMIT (4Fh)

The OT_FAULT_LIMIT is a standard PMBus™ command that allows configuring or reading the threshold for the Overtemperature Fault detection. Reading and writing to this register should use the coefficients shown in Table 41. Accesses to this command should use the PMBus™ read or write word protocol. If the measured temperature exceeds this value, an overtemperature fault is triggered, the MOSFET is switched off, OT Fault flags are set in the respective registers, and the SMBA signal is asserted. After the measured temperature falls below the value in this register, the MOSFET may be switched back on with the OPERATION command. A single temperature measurement is an average of 16 round-robin cycles. Therefore, the minimum temperature fault detection time is 16 ms.

Table 5. OT_FAULT_LIMIT Register

VALUE	MEANING	DEFAULT
0h – 0FFEh	Overtemperature fault threshold value	0960h (150°C)
0FFFh	Overtemperature fault detection disabled	–

8.5.1.1.6 OT_WARN_LIMIT (51h)

The OT_WARN_LIMIT is a standard PMBus™ command that allows configuring or reading the threshold for the Overtemperature Warning detection. Reading and writing to this register should use the coefficients shown in Table 41. Accesses to this command should use the PMBus™ read or write word protocol. If the measured temperature exceeds this value, an overtemperature warning is triggered, the OT Warn flags are set in the respective registers, and the SMBA signal is asserted. A single temperature measurement is an average of 16 round-robin cycles. Therefore, the minimum temperature warn detection time is 16 ms.

Table 6. OT_WARN_LIMIT Register

VALUE	MEANING	DEFAULT
0h – 0FFEh	Overtemperature warn threshold value	07D0h (125°C)
0FFFh	Overtemperature warn detection disabled	–

8.5.1.1.7 VIN_OV_WARN_LIMIT (57h)

The VIN_OV_WARN_LIMIT is a standard PMBus™ command that allows configuring or reading the threshold for the VIN Overvoltage Warning detection. Reading and writing to this register should use the coefficients shown in Table 41. Accesses to this command should use the PMBus™ read or write word protocol. If the measured value of VIN rises above the value in this register, VIN OV Warn flags are set in the respective registers, and the SMBA signal is asserted.

Table 7. VIN_OV_WARN_LIMIT Register

VALUE	MEANING	DEFAULT
0h – 0FFEh	VIN Overvoltage warning detection threshold	0FFFh (disabled)
0FFFh	VIN Overvoltage warning disabled	–

8.5.1.1.8 VIN_UV_WARN_LIMIT (58h)

The VIN_UV_WARN_LIMIT is a standard PMBus™ command that allows configuring or reading the threshold for the VIN Undervoltage Warning detection. Reading and writing to this register should use the coefficients shown in Table 41. Accesses to this command should use the PMBus™ read or write word protocol. If the measured value of VIN falls below the value in this register, VIN UV Warn flags are set in the respective registers, and the SMBA signal is asserted.

Table 8. VIN_UV_WARN_LIMIT Register

VALUE	MEANING	DEFAULT
1h – 0FFFh	VIN Undervoltage warning detection threshold	0000h (disabled)
0000h	VIN Undervoltage warning disabled	–

8.5.1.1.9 STATUS_BYTE (78h)

The STATUS_BYTE command is a standard PMBus™ command that returns the value of a number of flags indicating the state of the LM25066A. Accesses to this command should use the PMBus™ read byte protocol. To clear bits in this register, the underlying fault should be removed and a CLEAR_FAULTS command issued.

Table 9. STATUS_BYTE Definitions

BIT	NAME	MEANING	DEFAULT
7	BUSY	Not supported, always 0	0
6	OFF	This bit is asserted if the MOSFET is not switched on for any reason	1
5	VOUT OV	Not supported, always 0	0
4	IOUT OC	Not supported, always 0	0
3	VIN UV FAULT	A VIN undervoltage fault has occurred	1
2	TEMPERATURE	A temperature fault or warning has occurred	0
1	CML	A communication fault has occurred	0
0	None of the above	A fault or warning not listed in bits [7:1] has occurred	1

8.5.1.1.10 STATUS_WORD (79h)

The STATUS_WORD command is a standard PMBus™ command that returns the value of a number of flags indicating the state of the LM25066A. Accesses to this command should use the PMBus™ read word protocol. To clear bits in this register, the underlying fault should be removed and a CLEAR_FAULTS command issued. The INPUT and VIN UV FAULT flags will default to 1 on start-up. However, they will be cleared to 0 after the first time the input voltage exceeds the resistor programmed UVLO threshold.

Table 10. STATUS_WORD Definitions

BIT	NAME	MEANING	DEFAULT
15	VOUT	An output voltage fault or warning has occurred	0
14	IOUT/POUT	Not supported, always 0	0
13	INPUT	An input voltage or current fault has occurred	1
12	MFR	A manufacturer specific fault or warning has occurred	1
11	$\overline{\text{POWER GOOD}}$	The Power Good signal has been negated	1
10	FANS	Not supported, always 0	0
9	OTHER	Not supported, always 0	0
8	UNKNOWN	Not supported, always 0	0
7	BUSY	Not supported, always 0	0
6	OFF	This bit is asserted if the MOSFET is not switched on for any reason	1
5	VOUT OV	Not supported, always 0	0
4	IOUT OC	Not supported, always 0	0
3	VIN UV FAULT	A VIN undervoltage fault has occurred	1
2	TEMPERATURE	A temperature fault or warning has occurred	0
1	CML	A communication fault has occurred	0
0	None of the above	A fault or warning not listed in bits [7:1] has occurred	1

8.5.1.1.11 STATUS_VOUT (7Ah)

The STATUS_VOUT command is a standard PMBus™ command that returns the value of the VOUT UV Warning flag. Accesses to this command should use the PMBus™ read byte protocol. To clear bits in this register, the underlying fault should be removed and a CLEAR_FAULTS command issued.

Table 11. STATUS_VOUT Definitions

BIT	NAME	MEANING	DEFAULT
7	VOUT OV fault	Not supported, always 0	0
6	VOUT OV warn	Not supported, always 0	0
5	VOUT UV warn	A VOUT undervoltage warning has occurred	0
4	VOUT UV fault	Not supported, always 0	0
3	VOUT max	Not supported, always 0	0
2	TON max fault	Not supported, always 0	0
1	TOFF max fault	Not supported, always 0	0
0	VOUT tracking error	Not supported, always 0	0

8.5.1.1.12 STATUS_INPUT (7Ch)

The STATUS_INPUT command is a standard PMBus™ command that returns the value of a number of flags related to input voltage, current, and power. Accesses to this command should use the PMBus™ read byte protocol. To clear bits in this register, the underlying fault should be removed and a CLEAR_FAULTS command issued. The VIN UV Warn flag will default to 1 on start-up. However, it will be cleared to 0 after the first time the input voltage exceeds the resistor programmed UVLO threshold.

Table 12. STATUS_INPUT Definitions

BIT	NAME	MEANING	DEFAULT
7	VIN OV fault	A VIN overvoltage fault has occurred	0
6	VIN OV warn	A VIN overvoltage warning has occurred	0
5	VIN UV warn	A VIN undervoltage warning has occurred	1
4	VIN UV fault	A VIN undervoltage fault has occurred	0
3	Insufficient voltage	Not supported, always 0	0
2	IIN OC fault	An IIN overcurrent fault has occurred	0
1	IIN OC warn	An IIN overcurrent warning has occurred	0
0	PIN OP warn	A PIN over-power warning has occurred	0

8.5.1.1.13 STATUS_TEMPERATURE (7Dh)

The STATUS_TEMPERATURE is a standard PMBus™ command that returns the value of the of a number of flags related to the temperature telemetry value. Accesses to this command should use the PMBus™ read byte protocol. To clear bits in this register, the underlying fault should be removed and a CLEAR_FAULTS command issued.

Table 13. STATUS_TEMPERATURE Definitions

BIT	NAME	MEANING	DEFAULT
7	Overtemp fault	An overtemperature fault has occurred	0
6	Overtemp warn	An overtemperature warning has occurred	0
5	Undertemp warn	Not supported, always 0	0
4	Undertemp fault	Not supported, always 0	0
3	Reserved	Not supported, always 0	0
2	Reserved	Not supported, always 0	0
1	Reserved	Not supported, always 0	0
0	Reserved	Not supported, always 0	0

8.5.1.1.14 STATUS_CML (7Eh)

The STATUS_CML command is a standard PMBus™ command that returns the value of a number of flags related to communication faults. Accesses to this command should use the PMBus™ read byte protocol. To clear bits in this register, a CLEAR_FAULTS command should be issued.

Table 14. STATUS_CML Definitions

BIT	NAME	DEFAULT
7	Invalid or unsupported command received	0
6	Invalid or unsupported data received	0
5	Packet error check failed	0
4	Memory fault detected not supported, always 0	0
3	Processor fault detected not supported, always 0	0
2	Reserved not supported, always 0	0
1	Miscellaneous communications fault has occurred	0
0	Other memory or logic fault detected not supported, always 0	0

8.5.1.1.15 STATUS_MFR_SPECIFIC (80h)

The STATUS_MFR_SPECIFIC command is a standard PMBus™ command that contains manufacturer specific status information. Accesses to this command should use the PMBus™ read byte protocol. To clear bits in this register, the underlying fault should be removed and a CLEAR_FAULTS command should be issued.

Table 15. STATUS_MFR_SPECIFIC Definitions

BIT	MEANING	DEFAULT
7	Circuit breaker fault	0
6	Ext. MOSFET shorted fault	0
5	Not supported, always 0	0
4	Defaults loaded	1
3	Not supported, always 0	0
2	Not supported, always 0	0
1	Not supported, always 0	0
0	Not supported, always 0	0

8.5.1.1.16 READ_VIN (88h)

The READ_VIN command is a standard PMBus™ command that returns the 12-bit measured value of the input voltage. Reading this register should use the coefficients shown in Table 41. Accesses to this command should use the PMBus™ read word protocol. This value is also used internally for the VIN Over and Under Voltage Warning detection.

Table 16. READ_VIN Register

VALUE	MEANING	DEFAULT
0h – 0FFFh	Measured value for VIN	0000h

8.5.1.1.17 READ_VOUT (8Bh)

The READ_VOUT command is a standard PMBus™ command that returns the 12-bit measured value of the output voltage. Reading this register should use the coefficients shown in Table 41. Accesses to this command should use the PMBus™ read word protocol. This value is also used internally for the VOUT Under Voltage Warning detection.

Table 17. READ_VOUT Register

VALUE	MEANING	DEFAULT
0h – 0FFFh	Measured value for VOUT	0000h

8.5.1.1.18 READ_TEMPERATURE_1 (8Dh)

The READ_TEMPERATURE _1 command is a standard PMBus™ command that returns the signed value of the temperature measured by the external temperature sense diode. Reading this register should use the coefficients shown in Table 41. Accesses to this command should use the PMBus™ read word protocol. This value is also used internally for the Over Temperature Fault and Warning detection. This data has a range of -256°C to + 255°C after the coefficients are applied.

Table 18. READ_TEMPERATURE_1 Register

VALUE	MEANING	DEFAULT
0h – 0FFFh	Measured value for TEMPERATURE	0000h

8.5.1.1.19 MFR_ID (99h)

The MFR_ID command is a standard PMBus™ command that returns the identification of the manufacturer. To read the MFR_ID, use the PMBus™ block read protocol.

Table 19. MFR_ID Register

BYTE	NAME	VALUE
0	Number of bytes	03h
1	MFR ID-1	4Eh ‘N'
2	MFR ID-2	53h ‘S'
3	MFR ID-3	43h ‘C'

8.5.1.1.20 MFR_MODEL (9Ah)

The MFR_MODEL command is a standard PMBus™ command that returns the part number of the chip. To read the MFR_MODEL, use the PMBus™ block read protocol.

Table 20. MFR_MODEL Register

BYTE	NAME	VALUE
0	Number of bytes	08h
1	MFR ID-1	4Ch ‘L'
2	MFR ID-2	4Dh ‘M'
3	MFR ID-3	32h ‘2'
4	MFR ID-4	35h ‘5'
5	MFR ID-5	30h ‘0'
6	MFR ID-6	36h ‘6'
7	MFR ID-7	36h ‘6'
8	MFR ID-8	00h

8.5.1.1.21 MFR_REVISION (9Bh)

The MFR_REVISION command is a standard PMBus™ command that returns the revision level of the part. To read the MFR_REVISION, use the PMBus™ block read protocol.

Table 21. MFR_REVISION Register

BYTE	NAME	VALUE
0	Number of bytes	02h
1	MFR ID-1	41h ‘A'
2	MFR ID-2	41h ‘A'

8.5.1.2 Manufacturer Specific PMBus™ Commands

8.5.1.2.1 MFR_SPECIFIC_00: READ_VAUX (D0h)

The READ_VAUX command will report the 12-bit ADC measured auxiliary voltage. Voltages greater than or equal to 1.16 V to ground will be reported at plus full scale (0FFFh). Voltages less than or equal to 0 V referenced to ground will be reported as 0 (0000h). Coefficients for the VAUX value are dependent on the value of the external divider (if used). To read data from the READ_VAUX command, use the PMBus™ Read Word protocol.

Table 22. READ_VAUX Register

VALUE	MEANING	DEFAULT
0h – 0FFFh	Measured value for VAUX input	0000h

8.5.1.2.2 MFR_SPECIFIC_01: MFR_READ_IIN (D1h)

The MFR_READ_IIN command will report the 12-bit ADC measured current sense voltage. To read data from the MFR_READ_IIN command, use the PMBus™ Read Word protocol. Reading this register should use the coefficients shown in Table 41. See *Determining Telemetry Coefficients Empirically With Linear Fit* to calculate the values to use.

Table 23. MFR_READ_IIN Register

VALUE	MEANING	DEFAULT
0h – 0FFFh	Measured value for input current sense voltage	0000h

8.5.1.2.3 MFR_SPECIFIC_02: MFR_READ_PIN (D2h)

The MFR_ READ_PIN command will report the upper 12 bits of the VIN × IIN product as measured by the 12-bit ADC. To read data from the MFR_READ_PIN command, use the PMBus™ Read Word protocol. Reading this register should use the coefficients shown in Table 41. Please see the section on coefficient calculations to calculate the values to use.

Table 24. MFR_READ_PIN Register

VALUE	MEANING	DEFAULT
0h – 0FFFh	Value for input current × input voltage	0000h

8.5.1.2.4 MFR_SPECIFIC_03: MFR_IN_OC_WARN_LIMIT (D3h)

The MFR_IIN_OC_ WARN_LIMIT PMBus™ command sets the input overcurrent warning threshold. In the event that the input current rises above the value set in this register, the IIN overcurrent flags are set in the status registers and the $\overline{\text{SMBA}}$ is asserted. To access the MFR_IIN_ OC_WARN_LIMIT register, use the PMBus™ Read/Write Word protocol. Reading/writing to this register should use the coefficients shown in Table 41.

Table 25. MFR_IIN_OC_WARN_LIMIT Register

VALUE	MEANING	DEFAULT
0h – 0FFEh	Value for input overcurrent warn limit	0FFFh
0FFFh	Input overcurrent warning disabled	–

8.5.1.2.5 MFR_SPECIFIC_04: MFR_PIN_OP_WARN_LIMIT (D4h)

The MFR_PIN_OP_WARN_LIMIT PMBus™ command sets the input over-power warning threshold. In the event that the input power rises above the value set in this register, the PIN Over-power flags are set in the status registers and the $\overline{\text{SMBA}}$ is asserted. To access the MFR_PIN_OP_WARN_LIMIT register, use the PMBus™ Read/Write Word protocol. Reading/writing to this register should use the coefficients shown in Table 41.

Table 26. MFR_PIN_OP_WARN_LIMIT Register

VALUE	MEANING	DEFAULT
0h – 0FFEh	Value for input over-power warn limit	0FFFh
0FFFh	Input over-power warning disabled	–

8.5.1.2.6 MFR_SPECIFIC_05: READ_PIN_PEAK (D5h)

The READ_PIN_PEAK command will report the maximum input power measured since a Power-On-Reset or the last CLEAR_PIN_PEAK command. To access the READ_PIN_PEAK command, use the PMBus™ Read Word protocol. Use the coefficients shown in Table 41.

Table 27. READ_PIN_PEAK Register

VALUE	MEANING	DEFAULT
0h – 0FFEh	Maximum value for input current × input voltage since reset or last clear	0h

8.5.1.2.7 MFR_SPECIFIC_06: CLEAR_PIN_PEAK (D6h)

The CLEAR_PIN_PEAK command will clear the PIN_PEAK register. This command uses the PMBus™ Send Byte protocol.

8.5.1.2.8 MFR_SPECIFIC_07: GATE_MASK (D7h)

The GATE_MASK register allows the hardware to prevent fault conditions from switching off the MOSFET. When the bit is high, the corresponding FAULT has no control over the MOSFET gate. All status registers will still be updated (STATUS, DIAGNOSTIC) and an $\overline{\text{SMBA}}$ will still be issued. This register is accessed with the PMBus™ Read / Write Byte protocol.

WARNING

Inhibiting the MOSFET switch off in response to overcurrent or circuit breaker fault conditions will likely result in the destruction of the MOSFET. This functionality should be used with great care and supervision.

Table 28. GATE_MASK Register

BIT	NAME	DEFAULT
7	Not used, always 0	0
6	Not used, always 0	0
5	VIN UV FAULT	0
4	VIN OV FAULT	0
3	Not used, do not write to bit	0
2	OVERTEMP FAULT	0
1	Not used, always 0	0
0	Not used, do not write to bit	0

8.5.1.2.9 MFR_SPECIFIC_08: ALERT_MASK (D8h)

The ALERT_MASK is used to mask the $\overline{\text{SMBA}}$ when a specific fault or warning has occurred. Each bit corresponds to one of the 14 different analog and digital faults or warnings that would normally result in an $\overline{\text{SMBA}}$ being set. When the corresponding bit is high, that condition will not cause the $\overline{\text{SMBA}}$ to be asserted. If that condition occurs, the registers where that condition is captured will still be updated (STATUS registers, DIAGNOSTIC_WORD) and the external MOSFET gate control will still be active (VIN_OV_FAULT, VIN_UV_FAULT, IIN/PFET_FAULT, CB_FAULT, OT_FAULT). This register is accessed with the PMBus™ Read / Write Word protocol. The VIN UNDERVOLTGE FAULT flag will default to 1 on start-up. However, it will be cleared to 0 after the first time the input voltage exceeds the resistor programmed UVLO threshold.

Table 29. ALERT_MASK Definitions

BIT	NAME	DEFAULT
15	VOUT UNDERVOLTAGE WARN	0
14	IIN LIMIT warn	0
13	VIN UNDERVOLTAGE WARN	0
12	VIN OVERVOLTAGE WARN	0
11	$\overline{\text{POWER GOOD}}$	1
10	OVERTEMP WARN	0
9	Not used	0
8	OVERPOWER LIMIT WARN	0
7	Not used	0
6	EXT_MOSFET_SHORTED	0
5	VIN UNDERVOLTAGE FAULT	1
4	VIN OVERVOLTAGE FAULT	0
3	IIN/PFET FAULT	0
2	OVERTEMPERATURE FAULT	0
1	CML FAULT (communications fault)	0
0	CIRCUIT BREAKER FAULT	0

8.5.1.2.10 MFR_SPECIFIC_09: DEVICE_SETUP (D9h)

The DEVICE_SETUP command may be used to override pin settings to define operation of the LM25066A under host control. This command is accessed with the PMBus™ read / write byte protocol.

Table 30. DEVICE_SETUP Byte Format

BIT	NAME	MEANING
7:5	Retry setting	111 = Unlimited retries
		110 = Retry 16 times
		101 = Retry 8 times
		100 = Retry 4 times
		011 = Retry 2 times
		010 = Retry 1 time
		001 = No retries
		000 = Pin configured retries
4	Current limit setting	0 = Low setting (25 mV)
		1 = High setting (46 mV)
3	CB/CL ratio	0 = Low setting (1.8x)
		1 = High setting (3.6x)
2	Current limit configuration	0 = Use pin settings
		1 = Use SMBus settings
1	Circuit breaker configuration	0 = Use pin settings
		1 = Use SMBus settings
0	Unused	–

In order to configure the Current Limit Setting via this register, it is necessary to set the Current Limit Configuration bit (2) to 1 to enable the register to control the current limit function and the Current Limit Setting bit (4) to select the desired setting. Similarly, in order to control the Circuit Breaker via this register, it is necessary to set the Circuit Breaker Configuration bit (1) to 1 to enable the register to control the Circuit Breaker Setting, and the Circuit Breaker / Current Limit Ratio bit (3) to the desired value. If the respective Configuration bits are not set, the Settings will be ignored and the pin set values used.

The Current Limit Configuration effects the coefficients used for the Current and Power measurements and warning registers.

8.5.1.2.11 MFR_SPECIFIC_10: BLOCK_READ (DAh)

The BLOCK_READ command concatenates the DIAGNOSTIC_WORD with input and output telemetry information (IIN, VOUT, VIN, PIN) as well as TEMPERATURE to capture all of the operating information of the LM25066A in a single SMBus transaction. The block is 12 bytes long with telemetry information being sent out in the same manner as if an individual READ_XXX command had been issued (shown below). The contents of the block read register are updated every clock cycle (85 ns) as long as the SMBus interface is idle. BLOCK_READ also guarantees that the VIN, VOUT, IIN and PIN measurements are all time-aligned whereas there is a chance they may not be if read with individual PMBus™ commands.

The Block Read command is read via the PMBus™ block read protocol.

Table 31. BLOCK_READ Register Format

BYTE COUNT (ALWAYS 12)	(1 BYTE)
DIAGNOSTIC_WORD	(1 word)
IIN_BLOCK	(1 word)
VOUT_BLOCK	(1 word)
VIN_BLOCK	(1 word)
PIN_BLOCK	(1 word)
TEMP_BLOCK	(1 word)

8.5.1.2.12 MFR_SPECIFIC_11: SAMPLES_FOR_AVG (DBh)

The SAMPLES_FOR_AVERAGE is a manufacturer specific command for setting the number of samples used in computing the average values for IIN, VIN, VOUT, PIN. The decimal equivalent of the AVGN nibble is the power of 2 samples (for example, AVGN=12 equates to 4096 samples used in computing the average). The LM25066A supports average numbers of 1, 2, 4, 8, 16, 32, 64, 128, 256, 512, 1024, 2048, 4096. The SAMPLES_FOR_AVG number applies to average values of IIN, VIN, VOUT, PIN simultaneously. The LM25066A uses simple averaging. This is accomplished by summing consecutive results up to the number programmed, then dividing by the number of samples. Averaging is calculated according to the following sequence:

$$Y = (X_{(N)} + X_{(N-1)} + ... + X_{(0)}) / 2^{AVGN} \quad (1)$$

When the averaging has reached the end of a sequence (for example, 4096 samples are averaged), then a whole new sequence begins that will require the same number of samples (in this example, 4096) to be taken before the new average is ready.

Table 32. SAMPLES_FOR_AVG Register

AVGN	$N=2^N$ AVERAGES	AVERAGING/REGISTER UPDATE PERIOD (ms)
0000	1	1
0001	2	2
0010	4	4
0011	8	8
0100	16	16
0101	32	32
0110	64	64
0111	128	128
1000	256	256
1001	512	512
1010	1024	1024
1011	2048	2048
1100	4096	4096

Note that a change in the SAMPLES_FOR_AVG register will not be reflected in the average telemetry measurements until the present averaging interval has completed. The default setting for AVGN is 0000 and therefore the average telemetry will mirror the instantaneous telemetry until a value higher than zero is programmed.

The SAMPLES_FOR_AVG register is accessed via the PMBus™ read / write byte protocol.

Table 33. SAMPLES_FOR_AVG Register

VALUE	MEANING	DEFAULT
0h – 0Ch	Exponent (AVGN) for number of samples to average over	00h

8.5.1.2.13 MFR_SPECIFIC_12: READ_AVG_VIN (DCh)

The READ_AVG_VIN command will report the 12-bit ADC measured input average voltage. If the data is not ready, the returned value will be the previous averaged data. However, if there is no previously averaged data, the default value (0000h) will be returned. This data is read with the PMBus™ Read Word protocol. This register should use the coefficients shown in Table 41.

Table 34. READ_AVG_VIN Register

VALUE	MEANING	DEFAULT
0h – 0FFFh	Average of measured values for input voltage	0000h

8.5.1.2.14 MFR_SPECIFIC_13: READ_AVG_VOUT (DDh)

The READ_AVG_VOUT command will report the 12-bit ADC measured average output voltage. The returned value will be the default value (0000h) or previous data when the average data is not ready. This data is read with the PMBus™ Read Word protocol. This register should use the coefficients shown in Table 41.

Table 35. READ_AVG_VOUT Register

VALUE	MEANING	DEFAULT
0h – 0FFFh	Average of measured values for output voltage	0000h

8.5.1.2.15 MFR_SPECIFIC_14: READ_AVG_IIN (DEh)

The READ AVG_IIN command will report the 12-bit ADC measured current sense average voltage. The returned value will be the default value (0000h) or previous data when the average data is not ready. This data is read with the PMBus™ Read Word protocol. This register should use the coefficients shown in Table 41.

Table 36. READ_AVG_IIN Register

VALUE	MEANING	DEFAULT
0h – 0FFFh	Average of measured values for current sense voltage	0000h

8.5.1.2.16 MFR_SPECIFIC_15: READ_AVG_PIN (DFh)

The READ_AVG_PIN command will report the upper 12 bits of the average VIN × IIN product as measured by the 12-bit ADC. You will read the default value (0000h) or previous data when the average data is not ready. This data is read with the PMBus™ Read Word protocol. This register should use the coefficients shown in Table 41.

Table 37. READ_AVG_PIN Register

VALUE	MEANING	DEFAULT
0h – 0FFFh	Average of measured value for input voltage × input current sense voltage	0000h

8.5.1.2.17 MFR_SPECIFIC_16: BLACK_BOX_READ (E0h)

The BLACK_BOX_READ command retrieves the BLOCK_READ data which was latched in at the first assertion of SMBA. It is re-armed with the CLEAR_FAULTS command. It is the same format as the BLOCK_READ registers, the only difference being that its contents are updated with the SMBA edge rather than the internal clock edge. This command is read with the PMBus™ Block Read protocol.

8.5.1.2.18 MFR_SPECIFIC_17: READ_DIAGNOSTIC_WORD (E1h)

The READ_DIAGNOSTIC_WORD PMBus command will report all of the LM25066A faults and warnings in a single read operation. The standard response to the assertion of the SMBA signal of issuing multiple read requests to various status registers can be replaced by a single word read to the DIAGNOSTIC_WORD register. The READ_DIAGNOSTIC_WORD command should be read with the PMBus™ Read Word protocol. The DIAGNOSTIC_WORD is also returned in the BLOCK_READ, BLACK_BOX_READ, and AVG_BLOCK_READ operations.

Table 38. READ_DIAGNOSTIC_WORD Format

BIT	MEANING	DEFAULT
15	VOUT_UNDERVOLTAGE_WARN	0
14	IIN_OP_WARN	0
13	VIN_UNDERVOLTAGE_WARN	0
12	VIN_OVERVOLTAGE_WARN	0
11	$\overline{\text{POWER GOOD}}$	1
10	OVER_TEMPERATURE_WARN	0
9	TIMER_LATCHED_OFF	0
8	EXT_MOSFET_SHORTED	0
7	CONFIG_PRESET	1
6	DEVICE_OFF	1
5	VIN_UNDERVOLTAGE_FAULT	1
4	VIN_OVERVOLTAGE_FAULT	0
3	IIN_OC/PFET_OP_FAULT	0
2	OVER_TEMPERATURE_FAULT	0
1	CML_FAULT	0
0	CIRCUIT_BREAKER_FAULT	0

8.5.1.2.19 MFR_SPECIFIC_18: AVG_BLOCK_READ (E2h)

The AVG_BLOCK_READ command concatenates the DIAGNOSTIC_WORD with input and output average telemetry information (IIN, VOUT, VIN, PIN) as well as TEMPERATURE to capture all of the operating information of the part in a single PMBus™ transaction. The block is 12 bytes long with telemetry information being sent out in the same manner as if an individual READ_AVG_XXX command had been issued (shown below). AVG_BLOCK_READ also guarantees that the VIN, VOUT, PIN, and IIN measurements are all time-aligned whereas there is a chance they may not be if read with individual PMBus™ commands. To read data from the AVG_BLOCK_READ command, use the SMBus Block Read protocol.

Table 39. AVG_BLOCK_READ Register Format

BYTE COUNT (ALWAYS 12)	(1 BYTE)
DIAGNOSTIC_WORD	(1 word)
AVG_IIN	(1 word)
AVG_VOUT	(1 word)
AVG_VIN	(1 word)
AVG_PIN	(1 word)
TEMPERATURE	(1 word)

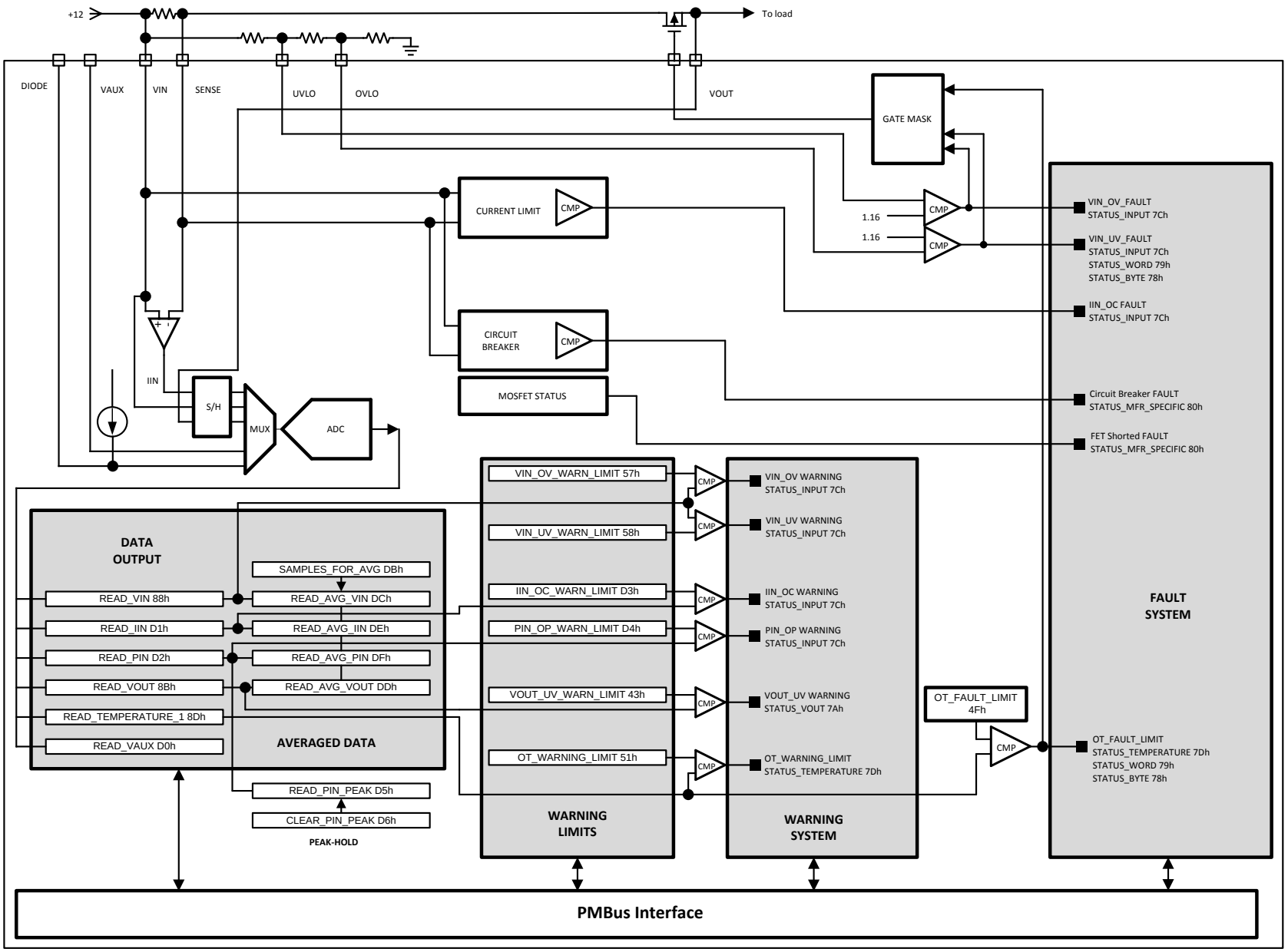


Figure 36. Command / Register and Alert Flow Diagram

8.5.1.3 Reading and Writing Telemetry Data and Warning Thresholds

All telemetry data is measured using a 12-bit ADC. This telemetry data and user programmed warning thresholds are communicated in 16-bit, two's compliment, signed data. This data is read or written in 2-byte increments conforming to the DIRECT format as described in section 8.3.3 of the PMBus™ Power System Management Protocol Specification 1.1 (Part II). The organization of the bits in the telemetry or warning word is shown in Table 40, where Bit_11 is the most significant bit (MSB) and Bit_0 is the least significant bit (LSB). The decimal equivalent of all warning and telemetry words are constrained to be within the range of 0 to 4095, with the exception of temperature. The decimal equivalent value of the temperature word ranges from 0 to 65535.

Table 40. Telemetry and Warning Word Format

BYTE	B7	B6	B5	B4	B3	B2	B1	B0
1	Bit_7	Bit_6	Bit_5	Bit_4	Bit_3	Bit_2	Bit_1	Bit_0
2	0	0	0	0	Bit_11	Bit_10	Bit_9	Bit_8

Conversion from direct format to real world dimensions of current, voltage, power, and temperature is accomplished by determining appropriate coefficients as described in section 7.2.1 of the PMBus™ Power System Management Protocol Specification 1.1 (Part II). According to this specification, the host system converts the values received into a reading of volts, amperes, watts, or other units using Equation 2:

$$X = \frac{1}{m}(Y \times 10^{-R} - b) \quad (2)$$

where

- **X:** the calculated "real world" value (volts, amps, watt, and so forth)
- **M:** the slope coefficient
- **Y:** a two byte two's complement integer received from device
- **B:** the offset, a two byte two's complement integer
- **R:** the exponent, a one byte two's complement integer
- R is only necessary in systems where m is required to be an integer (for example, where m may be stored in a register in an integrated circuit). In those cases, R only needs to be large enough to yield the desired accuracy.

Table 41. Telemetry and Warning Conversion Coefficients (R_S in mΩ)

COMMANDS	CONDITION	FORMAT	NUMBER OF DATA BYTES	M	B	R	UNIT
READ_VIN, READ_AVG_VIN VIN_OV_WARN_LIMIT VIN_UV_WARN_LIMIT		DIRECT	2	22070	–1800	–2	V
READ_VOUT, READ_AVG_VOUT VOUT_UV_WARN_LIMIT		DIRECT	2	22070	–1800	–2	V
READ_VAUX		DIRECT	2	3546	–3	0	V
*READ_IIN, READ_AVG_IIN MFR_IIN_OC_WARN_LIMIT	CL = GND	DIRECT	2	13661 × R_S	–5200	–2	A
*READ_IIN, READ_AVG_IIN MFR_IIN_OC_WARN_LIMIT	CL = VDD	DIRECT	2	6854 × R_S	–3100	–2	A
*READ_PIN, READ_AVG_PIN, READ_PIN_PEAK MFR_PIN_OP_WARN_LIMIT	CL = GND	DIRECT	2	736 × R_S	–3300	–2	W
*READ_PIN, READ_AVG_PIN, READ_PIN_PEAK MFR_PIN_OP_WARN_LIMIT	CL = VDD	DIRECT	2	369 × R_S	–1900	–2	W
READ_TEMPERATURE_1 OT_WARN_LIMIT OT_FAULT_LIMIT		DIRECT	2	16000	0	–3	°C

Care must be taken to adjust the exponent coefficient, R, such that the value of m remains within the range of –32768 to 32767. For example, if a 5-mΩ sense resistor is used, the correct coefficients for the READ_IIN command with CL = VDD would be m = 6830, b = –310, R = –1.

8.5.1.4 Determining Telemetry Coefficients Empirically With Linear Fit

The coefficients for telemetry measurements and warning thresholds presented in Table 41 are adequate for the majority of applications. Current and power coefficients must be calculated per application as they are dependent on the value of the sense resistor, RS, used. These were obtained by characterizing multiple units over temperature and are considered optimal. The small-signal nature of the current measurement make both current and power measurement more susceptible to PCB parasitics than other telemetry channels. In addition there is some variation in RS and the LM25066A itself. This may cause slight variations in the optimum coefficients (m, b, R) for converting from Direct Format digital values to real-world values (for example, amps and watts). To maximize telemetry accuracy, the coefficients can be calibrated for a given board using empirical methods. This would determine optimum coefficients to cancel out the error from PCB parasitics, RS variation, and the variation of the LM25066A. It is not considered good practice to take measurements on one board and use the computed coefficients for all units in production, because the RS and the LM25066A on a given board are randomly chosen and do not represent a statistical mean. It is recommended to either calibrate all boards individually or to use the recommended coefficients from Table 41.

The optimal current coefficients for a specific board can be determined using the following method:

1. While the LM25066A is in normal operation, measure the voltage across the sense resistor using kelvin test points and a high accuracy DVM while controlling the load current. Record the integer value returned by the READ_AVG_IIN command (with the SAMPLES_FOR_AVG set to a value greater than 0) for two or more voltages across the sense resistor. For best results, the individual READ_AVG_IIN measurements should span nearly the full scale range of the current (for example, voltage across R_S of 5 mV and 20 mV).
2. Convert the measured voltages to currents by dividing them by the value of R_S. For best accuracy, the value of R_S should be measured. Table 42 assumes a sense resistor value of 5 mΩ.

Table 42. Measurements for Linear Fit Determination of Current Coefficients

MEASURED VOLTAGE ACROSS R_S (V)	MEASURED CURRENT (A)	READ_AVG_IIN (INTERGER VALUE)
0.005	1	648
0.01	2	1331
0.02	4	2698

3. Using the spreadsheet or math program of your choice, determine the slope and the y-intercept values returned by the READ_AVG_IIN command versus the measured current. For the data shown in Table 42:
   – READ_AVG_IIN value = slope × (Measured Current) + (y-intercept)
   – slope = 683.4
   – y-intercept = -35.5
4. To determine the **M** coefficient, simply shift the decimal point of the calculated slope to arrive at an integer with a suitable number of significant digits for accuracy (typically 4) while staying with the range of -32768 to +32767. This shift in the decimal point equates to the **R** coefficient. For the slope value shown above, the decimal point would be shifted to the right once hence **R** = –1.
5. Once the **R** coefficient has been determined, the **B** coefficient is found by multiplying the y-intercept by 10^{-R}. In this case the value of **B** = –355.

   Calculated Current Coefficients:
   – **M** = 6834
   – **B** = -355
   – **R** = -1

$$X = \frac{1}{m}(Y \times 10^{-R} - b)$$

where

- **X:** the calculated real world value (volts, amps, watts, temperature)

- **M:** the slope coefficient, a the two byte two's complement integer
- **Y:** a two byte, two's complement integer received from device
- **B:** the offset, a two byte two's complement integer
- **R:** the exponent, a one byte two's complement integer
- The above procedure can be repeated to determine the coefficients of any telemetry channel simply by substituting measured current for some other parameter (for example, power, voltage, and so forth). (3)

8.5.1.5 Writing Telemetry Data

There are several locations that will require writing data if their optional usage is desired. Use the same coefficients previously calculated for your application and apply them using this method as prescribed by the *PMBus Power System Management Protocol Specification Part II – Command Language Revision 1.2, section 7.2.2*.

$$Y = (mX + b) \times 10^{R}$$

where

- **X:** the calculated real world value (volts, amps, watts, temperature)
- **M:** the slope coefficient, a two byte two's complement integer
- **Y:** a two byte two's complement integer received from device
- **B:** the offset, a two byte two's complement integer
- **R:** the exponent, a one byte two's complement integer (4)

8.5.1.6 PMBus™ Address Lines (ADR0, ADR1, ADR2)

The three address lines are to be set high (connect to VDD), low (connect to GND), or open to select one of 27 addresses for communicating with the LM25066A. Table 43 depicts 7-bit addresses (eighth bit is read/write bit).

Table 43. Device Addressing

ADR2	ADR1	ADR0	DECODED ADDRESS
Z	Z	Z	40h
Z	Z	0	41h
Z	Z	1	42h
Z	0	Z	43h
Z	0	0	44h
Z	0	1	45h
Z	1	Z	46h
Z	1	0	47h
Z	1	1	10h
0	Z	Z	11h
0	Z	0	12h
0	Z	1	13h
0	0	Z	14h
0	0	0	15h
0	0	1	16h
0	1	Z	17h
0	1	0	50h
0	1	1	51h
1	Z	Z	52h
1	Z	0	53h
1	Z	1	54h
1	0	Z	55h
1	0	0	56h
1	0	1	57h

Table 43. Device Addressing (continued)

ADR2	ADR1	ADR0	DECODED ADDRESS
1	1	Z	58h
1	1	0	59h
1	1	1	5Ah

8.5.1.7 $\overline{\text{SMBA}}$ Response

The $\overline{\text{SMBA}}$ effectively has two masks:

1. The Alert Mask Register at D8h, and
2. The ARA Automatic Mask.

The ARA Automatic Mask is a mask that is set in response to a successful ARA read. An ARA read operation returns the PMBus™ address of the lowest addressed part on the bus that has its $\overline{\text{SMBA}}$ asserted. A successful ARA read means that THIS part was the one that returned its address. When a part responds to the ARA read, it releases the $\overline{\text{SMBA}}$ signal. When the last part on the bus that has an $\overline{\text{SMBA}}$ set has successfully reported its address, the $\overline{\text{SMBA}}$ signal will de-assert.

The way that the LM25066A releases the $\overline{\text{SMBA}}$ signal is by setting the ARA Automatic mask bit for all fault conditions present at the time of the ARA read. All status registers will still show the fault condition, but it will not generate an $\overline{\text{SMBA}}$ on that fault again until the ARA Automatic mask is cleared by the host issuing a Clear Fault command to this part. This should be done as a routine part of servicing an $\overline{\text{SMBA}}$ condition on a part, even if the ARA read is not done. Figure 37 depicts a schematic version of this flow.

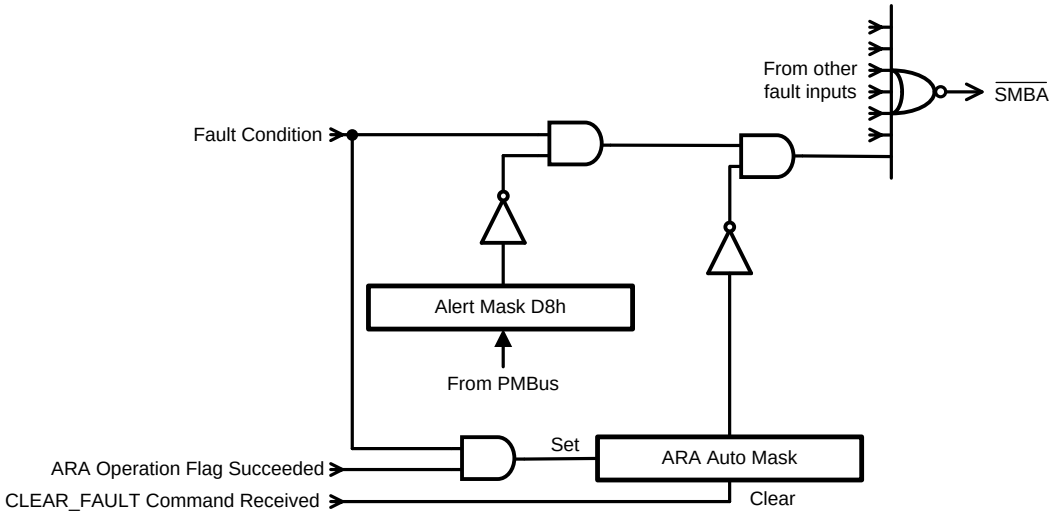


Figure 37. Typical Flow Schematic for $\overline{\text{SMBA}}$ Fault

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The LM25066A is a hot swap with a PMBus interface that provides current, voltage, power, and status information to the host. As a hot swap, it is used to manage inrush current and protect in case of faults.

When designing a hot swap, three key scenarios should be considered:

- Start-up
- Output of a hot swap is shorted to ground while the hot swap is on. This is often referred to as a hot-short.
- Powering-up a board when the output and ground are shorted. This is usually called a start-into-short.

All of these scenarios place a lot of stress on the hot swap MOSFET and thus special care is required when designing the hot swap circuit to keep the MOSFET operating within its SOA (Safe Operating Area). Detailed design examples are provided in the following sections. Solving all of the equations by hand is cumbersome and can result in errors. Instead, TI recommends using the LM25066A Design Calculator provided in *Development Support*.

9.2 Typical Application

9.2.1 12-V, 45-A PMBus Hotswap Design

This section describes the design procedure for a 12-V, 45-A PMBus hot swap design.

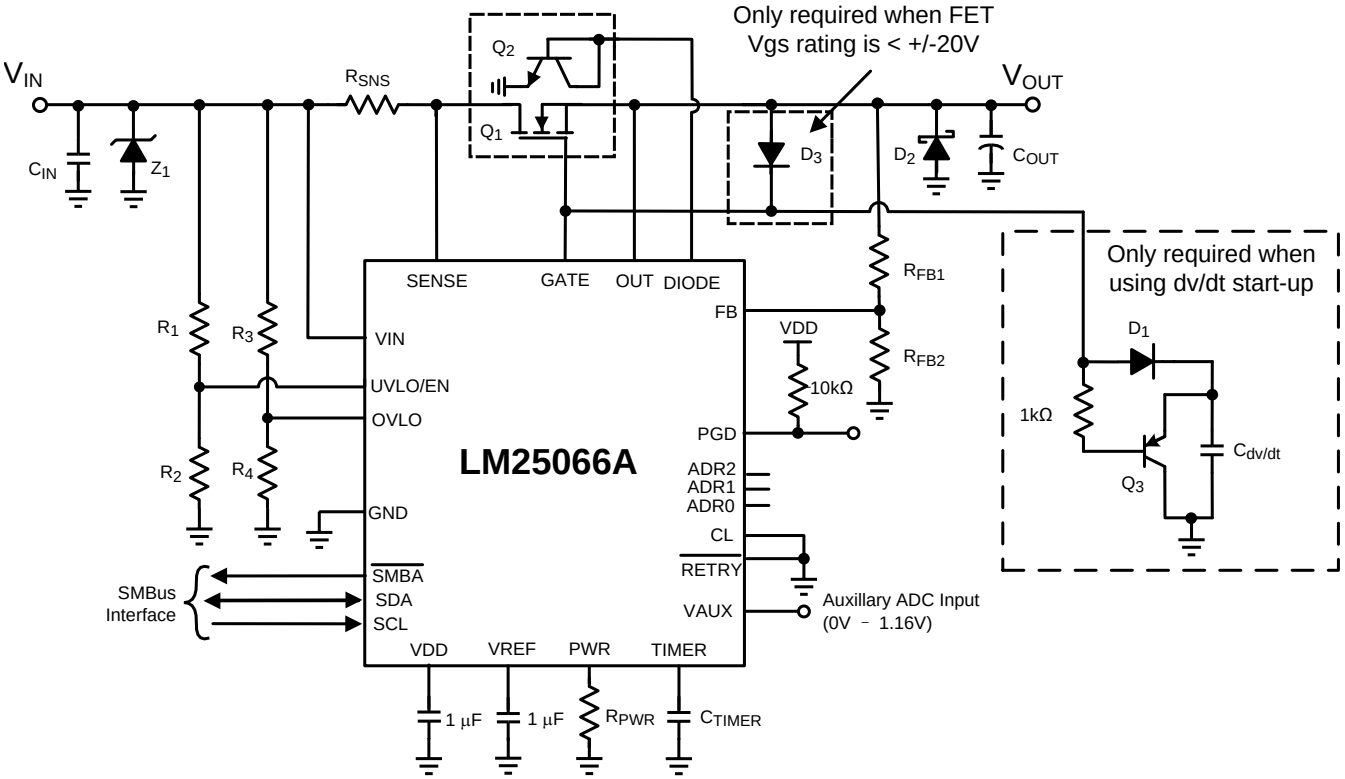


Figure 38. Typical Application Circuit

Typical Application (continued)

9.2.1.1 Design Requirements

Table 44 below summarizes the design parameters that must be known before designing a hot swap circuit. When charging the output capacitor through the hot swap MOSFET, the FET's total energy dissipation equals the total energy stored in the output capacitor (1/2 CV^2). Thus both the input voltage and Output capacitance will determine the stress experienced by the MOSFET. The maximum load current will drive the current limit and sense resistor selection. In addition, the maximum load current, maximum ambient temperature, and the thermal properties of the PCB ($R_{\theta CA}$) will drive the selection of the MOSFET R_{DSON} and the number of MOSFETs used. $R_{\theta CA}$ is a strong function of the layout and the amount of copper that is connected to the drain of the MOSFET. Note that the drain is not electrically connected to the ground plane and thus the ground plane cannot be used to help with heat dissipation. For this design example $R_{\theta CA}$ = 30 °C/W is used, which is similar to the LM25066A EVM. It's a good practice to measure the $R_{\theta CA}$ of a given design after the physical PCBs are available.

Finally, it's important to understand what test conditions the hot swap needs to pass. In general, a hot swap is designed to pass both a "Hot-Short" and a "Start into a Short", which are described in the previous section. Also it is recommended to keep the load OFF until the hot swap is fully powered up. Starting the load early will cause unnecessary stress on the MOSFET and could lead to MOSFET failures or a failure to start-up.

Table 44. Design Parameters

PARAMETER	EXAMPLE VALUE
Input voltage range	10 V to 14 V
Maximum load current	45 A
Maximum output capacitance of the hotswap	5600 µF
Maximum ambient temperature	55°C
MOSFET $R_{\theta CA}$ (function of layout)	30°C/W
Pass hot-short on output?	Yes
Pass a start into short?	Yes
Is the load off until PG asserted?	Yes
Can a hot board be plugged back in?	Yes

9.2.1.2 Detailed Design Procedure

9.2.1.2.1 Select R_{SNS} and CL Setting

LM25066A can be used with a VCL of 25 mV or 46 mV. In general using the 25-mV threshold will result in a lower RSNS and lower I^2R losses. This option is selected for this design by connecting the CL pin directly to VDD. It is recommended to target a current limit that is at least 10% above the maximum load current to account for the tolerance of the LM25066A current limit. Targeting a current limit of 50 A the sense resistor can be calculated using Equation 5:

$$R_{SNS,CLC} = \frac{V_{CL}}{I_{LIM}} = \frac{25\ mV}{50\ A} = 0.50\ m\Omega \quad (5)$$

Typically sense resistors are only available in discrete values. If a precise current limit is desired, a sense resistor along with a resistor divider can be used as shown in Figure 39.

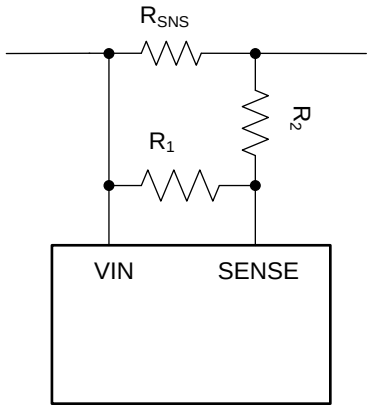


Figure 39. SENSE Resistor Divider

If using a resistor divider, then the next larger available sense resistor should be chosen (1 mΩ for example). The ratio of R1 and R2 can then be calculated using Equation 6:

$$\frac{R_1}{R_2} = \frac{R_{SNS,CLC}}{R_{SNS} - R_{SNS,CLC}} = \frac{0.5\,m\Omega}{1\,m\Omega - 0.5\,m\Omega} = 1 \quad (6)$$

Note that the SENSE pin will pull 25 μA of current, which will create an offset across R2. It is recommended to keep R2 below 10 Ω to reduce the offset that this introduces. In addition the 1% resistors will add to the current monitoring error. Finally, if the resistor divider approach is used, the user should compute the effective sense resistance ($R_{SNS,EFF}$) using Equation 7 and use that in all equations instead of R_{SNS}.

$$R_{SNS,EFF} = \frac{R_{SNS} \times R_1}{R_1 + R_2} \quad (7)$$

Note that for many applications, a precise current limit may not be required. In that case, it's simpler to pick the next smaller available sense resistor. For this application, a 0.5-mΩ resistor can be used for a 50 A current limit.

9.2.1.2.2 Selecting the Hotswap FETs

It is critical to select the correct MOSFET for a hot swap design. The device must meet the following requirements:

- The V_{DS} rating should be sufficient to handle the maximum system voltage along with any ringing caused by transients. For most 12-V systems a 30-V FET is a good choice.
- The SOA of the FET should be sufficient to handle all usage cases: start-up, hot-short, start into short.
- R_{DSON} should be sufficiently low to maintain the junction and case temperature below the maximum rating of the FET. In fact, it is recommended to keep the steady state FET temperature below 125°C to allow margin to handle transients.
- Maximum continuous current rating should be above the maximum load current and the pulsed drain current must be greater than the current threshold of the circuit breaker. Most MOSFETs that pass the first three requirements will also pass these two.
- A V_{GS} rating of ± 20 V is required, because the LM25066A can pull up the gate as high as 16 V above source.
  - Otherwise, a diode (D3 in Figure 38) can be used to protect MOSFETs with a ± 12 V V_{GS} rating.

For this design the CSD17556Q5B was selected for its low R_{DSON} and good SOA. After selecting the MOSFET, the maximum steady state case temperature can be calculated using Equation 8:

$$T_{C,MAX} = T_{A,MAX} + R_{\theta CA} \times I^2_{LOAD,MAX} \times R_{DSON}(T_J) \quad (8)$$

Note that the R_{DSON} is a strong function of junction temperature, which for most MOSFETs will be close to the case temperature. A few iterations of the above equations may be necessary to converge on the final R_{DSON} and $T_{C,MAX}$ value. According to the CSD17556Q5B datasheet, its R_{DSON} is approximately 1.3x at 85°C. Equation 9 uses this R_{DSON} value to compute the $T_{C,MAX}$.

$$T_{C,MAX} = 55°C + 30° \frac{C}{W} \times (45\ A)^2 \times (1.3 \times 1.4\ m\Omega) = 165.6°C \quad (9)$$

This maximum steady state case temperature indicates that a second MOSFET may be needed to reduce and distribute power dissipation during normal operation. When using parallel MOSFETs, the maximum steady state case temperature can be calculated using Equation 10:

$$T_{C,MAX} = T_{A,MAX} + R_{\theta CA} \times \left(\frac{I_{LOAD,MAX}}{\#\ of\ MOSFETs} \right)^2 \times R_{DSON}(T_J) \quad (10)$$

Thus using two of the CSD17556Q5B in parallel will result in a steady state temperature of:

$$T_{C,MAX} = 55°C + 30° \frac{C}{W} \times \left(\frac{45\ A}{2} \right)^2 \times (1.3 \times 1.4\ m\Omega) = 82.6°C \quad (11)$$

Note that the computed $T_{C,MAX}$ is close to the junction temperature assumed for R_{DSON}. Thus no further iterations are necessary.

9.2.1.2.3 Select Power Limit

In general, a lower power limit setting is preferred to reduce the stress on the MOSFET. However, when the LM25066A is set to a very low power limit setting, it has to regulate the FET current and hence the voltage across the sense resistor (V_{SNS}) to a very low value. V_{SNS} can be calculated using Equation 12:

$$V_{SNS} = \frac{P_{LIM} \times R_{SNS}}{V_{DS}} \quad (12)$$

To avoid significant degradation of the power limiting a V_{SNS} of less than 4 mV is not recommended. Based on this requirement the minimum allowed power limit can be calculated using Equation 13:

$$P_{LIM,MIN} = \frac{V_{SNS,MIN} \times V_{IN,MAX}}{R_{SNS}} = \frac{4\ mV \times 14\ V}{0.5\ m\Omega} = 112\ W \quad (13)$$

In most applications the power limit can be set to $P_{LIM,MIN}$ using Equation 14. Here R_{SNS} and R_{PWR} are in Ωs and P_{LIM} is in Watts.

$$R_{PWR} = 1.94 \times 10^5 \times R_{SNS} \left(P_{LIM} - 2.1\ mV \times \frac{V_{DS}}{R_{SNS}} \right) \quad (14)$$

So note that the minimum R_{PWR} would occur when $V_{DS} = V_{IN,MAX}$. We can then calculate the minimum R_{PWR} using Equation 15:

$$R_{PWR} = 1.94 \times 10^5 \times 0.5\ m\Omega \left(112\ W - 2.1\ mV \times \frac{14\ V}{0.5\ m\Omega} \right) = 5.16\ k\Omega \quad (15)$$

The next largest available resistor should be selected. In this case a 5.23-kΩ resistor was chosen, which sets a 112.72 W power limit.

9.2.1.2.4 Set Fault Timer

The fault timer runs when the hot swap is in power limit or current limit, which is the case during start-up. Thus the timer has to be sized large enough to prevent a time-out during start-up. If the device starts directly into current limit (I_{LIM}) × V_{DS} < P_{LIM}) the maximum start time can be calculated using Equation 16:

$$t_{start,max} = \frac{C_{OUT} \times V_{IN,MAX}}{I_{LIM}} \quad (16)$$

For most designs (including this example) $I_{LIM} \times V_{DS} > P_{LIM}$ so the hot swap will start in power limit and transition into current limit. In that case the estimated start time can be calculated using Equation 17:

$$t_{start} = \frac{C_{OUT}}{2} \times \left[\frac{V_{IN,MAX}^2}{P_{LIM}} + \frac{P_{LIM}}{I_{LIM}^2} \right] = \frac{5600\ \mu F}{2} \times \left[\frac{(14\ V)^2}{112\ W} + \frac{112\ W}{(50\ A)^2} \right] = 5.03\ ms \quad (17)$$

Note that the above start-time assumes constant, typical current limit and power limit values. The actual start-up time will be slightly longer, as the power limit is a function of V_{DS} and will decrease as the output voltage increases. To ensure that the timer never times out during start-up, it is recommended to set the fault time (t_{flt}) to be 2 × $t_{star}t$ or 10.06 ms. This will account for the variation in power limit, timer current, and timer capacitance. Thus C_{TIMER} can be calculated using Equation 18:

$$C_{TIMER} = \frac{t_{flt} \times i_{timer}}{V_{timer}} = \frac{10.06\ ms \times 90\ \mu A}{1.7\ V} = 533\ nF \tag{18}$$

The next largest available C_{TIMER} is chosen as 560 nF. Once the C_{TIMER} is chosen the actual programmed fault time can be calculated using Equation 19:

$$t_{flt} = \frac{C_{TIMER} \times v_{timer}}{i_{timer}} = \frac{560\ nF \times 1.7\ V}{90\ \mu A} = 10.58\ ms \tag{19}$$

9.2.1.2.5 Check MOSFET SOA

Once the power limit and fault timer are chosen, it's critical to check that the FET will stay within its SOA during all test conditions. During a "Hot-Short" the circuit breaker will trip and the LM25066A will restart into power limit until the timer runs out. In the worst case the MOSFET's V_{DS} will equal $V_{IN,MAX}$, I_{DS} will equal P_{LIM} / $V_{IN,MAX}$ and the stress event will last for t_{flt}. For this design example the MOSFET will have 14 V, 8 A across it for 10.58 ms.

Based on the SOA of the CSD17556Q5B, it can handle 14 V, 10 A for 10 ms and it can handle 14 V, 3 A for 100 ms. The SOA for 10.58 ms can be extrapolated by approximating SOA vs time as a power function as shown in Equation 20 through Equation 23:

$$I_{SOA}(t) = a \times t^{m} \tag{20}$$

$$m = \frac{\ln(I_{SOA}(t_1) / I_{SOA}(t_2)}{\ln(t_1 / t_2)} = \frac{\ln\left(\frac{10\ A}{3\ A}\right)}{\ln\left(\frac{10\ ms}{100\ ms}\right)} = -0.523 \tag{21}$$

$$a = \frac{I_{SOA}(t_1)}{t_1^{m}} = \frac{10\ A}{(10\ ms)^{-0.523}} = 10\ A \times (10\ ms)^{0.523} \tag{22}$$

$$I_{SOA}(10.58\ ms) = 10\ A \times (10\ ms)^{0.523} \times (10.58\ ms)^{-0.523} = 9.71\ A \tag{23}$$

Note that the SOA of a MOSFET is specified at a case temperature of 25°C, while the case temperature can be much hotter during a hot-short. The SOA should be de-rated based on $T_{C,MAX}$ using Equation 24:

$$I_{SOA}(10.58\ ms, T_{C,MAX}) = I_{SOA}(10.58\ ms, 25°C) \times \frac{T_{J,ABSMAX} - T_{C,MAX}}{T_{J,ABSMAX} - 25°C}$$

$$= 9.71\ A \times \frac{150°C - 82.6°C}{150°C - 25°C} = 5.24\ A \tag{24}$$

Based on this calculation the MOSFET can handle 5.24 A, 14 V for 10.58 ms at elevated case temperature, but is required to handle 8 A during a hot-short. This means the MOSFET will be at risk of getting damaged during a hot-short. In general, it is recommended for the MOSFET to be able to handle a minimum of 1.3x more power than what is required during a hot-short in order to provide margin to cover the variance of the power limit and fault time.

9.2.1.2.6 Switching to dV/dt based Start-up

For designs with large load currents and output capacitances, using a power limit based start-up can be impractical. Fundamentally, increasing load currents will reduce the sense resistor, which will increase the minimum power limit. Using a larger output capacitor will result in a longer start-up time and require a longer fault timer. Thus a longer fault timer and a larger power limit setting are required, which places more stress on the MOSFET during a hot-short or a start into short. Eventually, there will be no FETs that can support such a requirement.

To avoid this problem, a dV/dt limiting capacitor ($C_{dV/dt}$) can be used to limit the slew rate of the gate and the output voltage. The inrush current can be set arbitrarily small by reducing the slew rate of the V_{OUT}. In addition, the power limit is set to satisfy the minimum power limit requirement and to keep the timer from running during start-up (make P_{LIM} / $V_{IN,MAX}$ > I_{INR}). Since the timer doesn't run during start-up it can be made small to reduce the stress that the MOSFET experiences during a start into short or a hot-short.

The D2 prevents the charge of $C_{dV/dt}$ from interfering with the power limit loop during a hot-short event and Q3 discharges $C_{dV/dt}$ when the hot swap gate comes down.

9.2.1.2.7 Choosing the VOUT Slew Rate

The inrush current should be kept low enough to keep the MOSFET within its SOA during start-up. Note that the total energy dissipated in the MOSFET during start-up is constant regardless of the inrush time. Thus, stretching it out over a longer time will always reduce the stress on the MOSFET as long as the load is off during start-up.

When choosing a target slew rate, one should pick a reasonable number, check the SOA and reduce the slew rate if necessary. Using 0.25 V/ms as a starting point the inrush current can be computed as follows:

$$I_{INR} = C_{OUT} \times \frac{dV_{OUT}}{dt} = 5600\ \mu F \times \frac{0.25\ V}{ms} = 1.4\ A \tag{25}$$

Assuming a maximum input voltage of 14 V, it will take 56 ms to start-up. Note that the power dissipation of the FET will start at $V_{IN,MAX}$ × I_{INR} and reduce to zero as the V_{DS} of the MOSFET is reduced. Note that the SOA curves assume the same power dissipation for a given time. A conservative approach is to assume an equivalent power profile where P_{FET} = $V_{IN,MAX}$ × I_{INR} for t = $t_{start\text{-}up}$ /2. In this instance, the SOA can be checked by looking at a 14 V, 1.4 A, 28 ms pulse. Using the same technique as *Check MOSFET SOA*, the MOSFET SOA can be estimated with Equation 26.

$$I_{SOA}(28\ ms) = 10\ A \times (10\ ms)^{0.523} \times (28\ ms)^{-0.523} = 5.84\ A \tag{26}$$

This value has to also be derated for temperature. For this calculation, it is assumed that T_C can equal $T_{A,MAX}$ when the board is plugged in. This would occur if a board is plugged in at an elevated ambient temperature environment.

$$I_{SOA}(28\ ms, T_{A,MAX}) = I_{SOA}(28\ ms, 25°C) \times \frac{T_{J,ABSMAX} - T_{A,MAX}}{T_{J,ABSMAX} - 25°C} = 5.84\ A \times \frac{150°C - 55°C}{150°C - 25°C} = 4.44\ A \tag{27}$$

Based on this calculation the MOSFET can handle 4.44 A, 14 V for 28 ms at elevated ambient temperature, and is required to handle 1.4 A. This indicates the MOSFET will stay well-within its SOA during a start-up if the slew rate is 0.25 V/ms or less. Note that if the load is off during start-up, the total energy dissipated in the FET is constant regardless of the slew rate. Thus a lower slew rate will always place less stress on the FET. To ensure that the slew rate is at most 0.25 V/ms the CdV/dt should be chosen with Equation 28.

$$c_{dV/dt} = \frac{I_{SOURCE,MAX}}{0.25\ V/ms} = \frac{22\ \mu A}{0.25\ V/ms} = 88\ nF \tag{28}$$

The next largest available $C_{dV/dt}$ is chosen to be 100 nF. Then the typical slew rate and start time can be computed to be 0.22 V/ms as shown below, making the typical start time 55 ms, assuming 12 V input.

$$V_{OUT,dV/dt} = \frac{I_{SOURCE}}{C_{dv/dt}} = \frac{22\ \mu A}{100\ nF} = 0.22\ V/ms \tag{29}$$

In certain applications, $T_{C,MAX}$ may be used for temperature derating instead. This would only occur if a hot board is unplugged and then plugged back in before it cools off to ambient temperature. This is worst case and for many applications, the $T_{A,MAX}$ can be used for this derating.

$$I_{SOA}(28\ ms, T_{C,MAX}) = I_{SOA}(28\ ms, 25°C) \times \frac{T_{J,ABSMAX} - T_{C,MAX}}{T_{J,ABSMAX} - 25°C} = 5.84\ A \times \frac{150°C - 82.6°C}{150°C - 25°C} = 3.15\ A \tag{30}$$

Based on this calculation using $T_{C,MAX}$ for derating, the MOSFET can handle 3.15 A, 14 V for 28 ms at elevated case temperature, and is required to handle 1.4 A. This indicates the MOSFET will stay well-within its SOA during a start-up if the slew rate is 0.25 V/ms or less.

9.2.1.2.8 Select Power Limit and Fault Timer

When picking the power limit, it needs to meet 2 requirements:

1. Power limit is large enough to avoid operating with V_{SNS} < 4 mV
2. Power limit is large enough to ensure that the timer doesn't run during start up. Picking a power limit such that it is 2x of $I_{INR,MAX} \times V_{IN,MAX}$ is good practice.

Thus the minimum allowed power limit can be computed with Equation 31.

$$P_{LIM,MIN} = \max\left(\frac{V_{SNS,MIN} \times V_{IN,MAX}}{R_{SNS}}, 2 \times V_{IN,MAX} \times I_{INR,MAX}\right) = \max(112\ W, 39.2\ W) = 112\ W \tag{31}$$

Next, the power limit is set to PLIM,MIN using the equation below. Here RSNS and RPWR are in Ωs and PLIM is in Watts.

$$R_{PWR} = 1.94 \times 10^5 \times R_{SNS}\left(P_{LIM} - 2.1\,mV \times \frac{Vds}{R_{SNS}}\right)$$

$$= 1.94 \times 10^5 \times 0.5\,m\Omega\left(112\ W - 2.1\,mV \times \frac{14\ V}{0.5\,m\Omega}\right) = 5.16\ k\Omega \tag{32}$$

The closest available resistor should be selected. In this case a 5.23-kΩ resistor was chosen.

Next a fault timer value should be selected. In general, the timer value should be decreased until there is enough margin between available SOA and the power pulse the FET experiences during a hot-short. For this design a 22-nF CTIMER was chosen corresponding to a 420-µs fault time. The available SOA is extrapolated using the method described earlier.

$$I_{SOA}(t) = a \times t^m \tag{33}$$

$$m = \frac{\ln(I_{SOA}(t_1)/I_{SOA}(t_2)}{\ln(t_1/t_2)} = \frac{\ln\left(\frac{100\ A}{30\ A}\right)}{\ln\left(\frac{0.1\,ms}{1\,ms}\right)} = -0.52 \tag{34}$$

$$a = \frac{I_{SOA}(t_2)}{t_2^m} = \frac{30\ A}{(1\,ms)^{-0.52}} = 30\ A \times (ms)^{0.52} \tag{35}$$

$$I_{SOA}(0.52\ ms, 25°C) = 30\ A \times (ms)^{0.52} \times (0.52\ ms)^{-0.52} = 42.3\ A \tag{36}$$

Next the available SOA is derated for temperature:

$$I_{SOA}\left(0.52ms, T_{C,MAX}\right) = 42.3A \times \frac{175°C - 114°C}{175°C - 25°C} = 17.17A \tag{37}$$

Note that only 4 A was required, while the FET can support 17.17A. This confirms that the design will be robust and have plenty of margin.

9.2.1.2.9 Set Undervoltage and Overvoltage Threshold

By programming the UVLO and OVLO thresholds the LM25066A enables the series pass device (Q_1) when the input supply voltage (V_{SYS}) is within the desired operational range. If V_{SYS} is below the UVLO threshold, or above the OVLO threshold, Q_1 is switched off, denying power to the load. Hysteresis is provided for each threshold.

9.2.1.2.9.1 Option A

The configuration shown in Figure 40 requires three resistors (R1-R3) to set the thresholds.

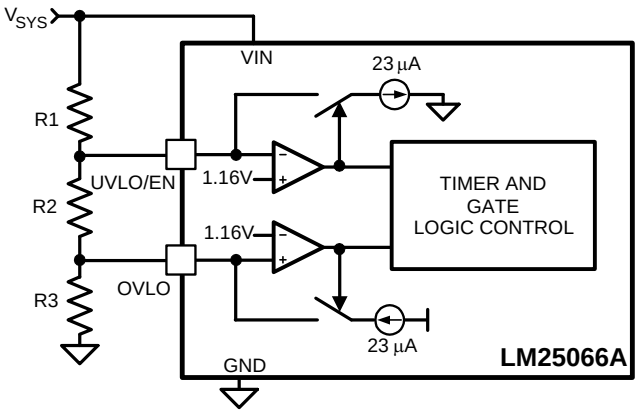


Figure 40. UVLO and OVLO Thresholds Set By R1-R3

The procedure to calculate the resistor values is as follows:

- Choose the upper UVLO threshold (V_{UVH}), and the lower UVLO threshold (V_{UVL}).
- Choose the upper OVLO threshold (V_{OVH}).
- The lower OVLO threshold (V_{OVL}) cannot be chosen in advance in this case, but is determined after the values for R1-R3 are determined. If V_{OVL} must be accurately defined in addition to the other three thresholds, see Option B below. The resistors are calculated as follows:

$$R1 = \frac{V_{UVH} - V_{UVL}}{23\ \mu A} = \frac{V_{UV(HYS)}}{23\ \mu A} \quad (38)$$

$$R3 = \frac{1.16V \times R1 \times V_{UVL}}{V_{OVH} \times (V_{UVL} - 1.16V)} \quad (39)$$

$$R2 = \frac{1.16V \times R1}{V_{UVL} - 1.16V} - R3 \quad (40)$$

The lower OVLO threshold is calculated from:

$$V_{OVL} = [(R1 + R2) \times (\frac{(1.16V)}{R3} - 23\ \mu A)] + 1.16V \quad (41)$$

As an example, assume the application requires the following thresholds: V_{UVH} = 8 V, V_{UVL} = 7 V, V_{OVH} = 15 V.

$$R1 = \frac{8V - 7V}{23\ \mu A} = \frac{1V}{23\ \mu A} = 43.5\ k\Omega \quad (42)$$

$$R3 = \frac{1.16V \times R1 \times 7V}{15V \times (7V - 1.16V)} = 4.03\ k\Omega \quad (43)$$

$$R2 = \frac{1.16V \times R1}{(7V - 1.16V)} - R3 = 4.61\ k\Omega \quad (44)$$

The lower OVLO threshold calculates to 12.03 V and the OVLO hysteresis is 2.97 V. Note that the OVLO hysteresis is always slightly greater than the UVLO hysteresis in this configuration. When the R1-R3 resistor values are known, the threshold voltages and hysteresis are calculated from the following:

$$V_{UVH} = 1.16V + [R1 \times (23\ \mu A + \frac{1.16V}{(R2 + R3)})] \quad (45)$$

$$V_{UVL} = \frac{1.16V \times (R1 + R2 + R3)}{R2 + R3} \quad (46)$$

$$V_{UV(HYS)} = R1 \times 23\ \mu A \quad (47)$$

$$V_{OVH} = \frac{1.16V \times (R1 + R2 + R3)}{R3} \quad (48)$$

$$V_{OVL} = [(R1 + R2) \times (\frac{1.16V}{R3} - 23\ \mu A)] + 1.16V \quad (49)$$

$$V_{OV(HYS)} = (R1 + R2) \times 23\mu A \quad (50)$$

9.2.1.2.9.2 Option B

If all four thresholds must be accurately defined, the configuration in Figure 41 can be used.

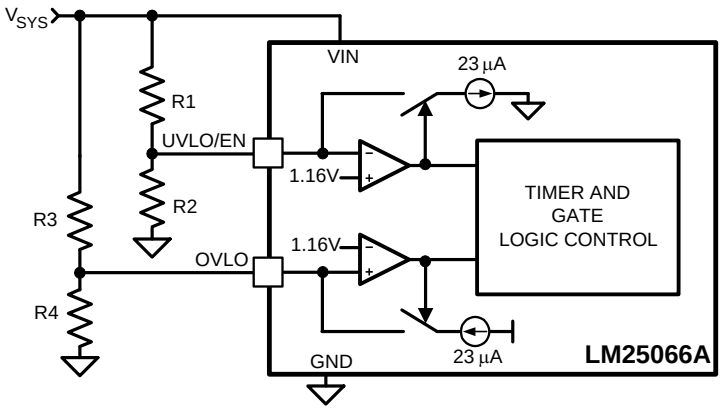


Figure 41. Programming the Four Thresholds

The four resistor values are calculated as follows:

- Choose the upper and lower UVLO thresholds (V_{UVH}) and (V_{UVL}).

$$R1 = \frac{V_{UVH} - V_{UVL}}{23\ \mu A} = \frac{V_{UV(HYS)}}{23\ \mu A} \quad (51)$$

$$R2 = \frac{1.16V \times R1}{(V_{UVL} - 1.16V)} \quad (52)$$

- Choose the upper and lower OVLO threshold (V_{OVH}) and (V_{OVL}).

$$R3 = \frac{V_{OVH} - V_{OVL}}{23\ \mu A} = \frac{V_{OV(HYS)}}{23\ \mu A} \quad (53)$$

$$R4 = \frac{1.16V \times R3}{(V_{OVH} - 1.16V)} \quad (54)$$

As an example, assume the application requires the following thresholds: V_{UVH} = 8 V, V_{UVL} = 7 V, V_{OVH} = 15.5 V, and V_{OVL} = 14 V. Therefore $V_{UV(HYS)}$ = 1 V and $V_{OV(HYS)}$ = 1.5 V. The resistor values are:

R1 = 43.5 kΩ, R2 = 8.64 kΩ (55)

R3 = 65.2 kΩ, R4 = 5.27 kΩ (56)

When the R1-R4 resistor values are known, the threshold voltages and hysteresis are calculated from the following:

$$V_{UVH} = 1.16V + [R1 \times (\frac{1.16V}{R2} + 23\ \mu A)] \quad (57)$$

$$V_{UVL} = \frac{1.16V \times (R1 + R2)}{R2} \quad (58)$$

$$V_{UV(HYS)} = R1 \times 23\ \mu A \quad (59)$$

$$V_{OVH} = \frac{1.16V \times (R3 + R4)}{R4} \quad (60)$$

$$V_{OVL} = 1.16V + [R3 \times (\frac{1.16V}{R4} - 23\ \mu A)] \quad (61)$$

$$V_{OV(HYS)} = R3 \times 23\ \mu A \quad (62)$$

9.2.1.2.9.3 Option C

The minimum UVLO level is obtained by connecting the UVLO/EN pin to VIN as shown in Figure 42. Q_1 is switched on when the VIN voltage reaches the POR threshold (≅ 2.6 V). The OVLO thresholds are set using R3, R4. Their values are calculated using the procedure in *Option B*.

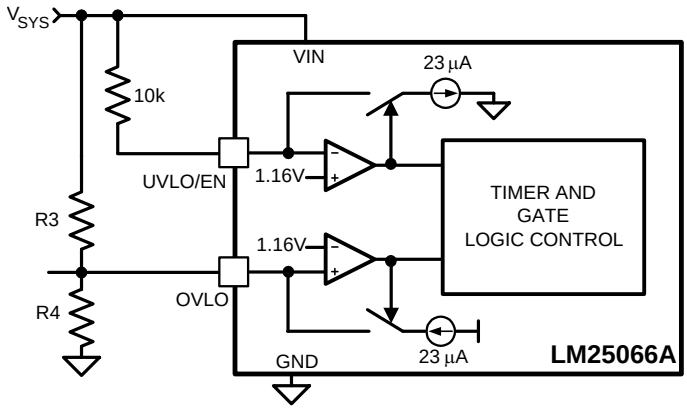


Figure 42. UVLO = POR

9.2.1.2.9.4 Option D

The OVLO function can be disabled by grounding the OVLO pin. The UVLO thresholds are set as described in *Option B* or *Option C*.

For this design example option B is used and the following values are targeted: VUVH = 10 V, VUVL = 9 V, VOVH = 15 V, VOVL = 14 V. R1, R2, R3, and R4 are computed using the equations below:

$$R1 = \frac{V_{UVH} - V_{UVL}}{23\ \mu A} = \frac{10\ V - 9\ V}{23\ \mu A} = 43.48\ k\Omega \quad (63)$$

$$R2 = \frac{1.16\ V \times R1}{(V_{UVL} - 1.16\ V)} = \frac{1.16\ V \times 43.48\ k\Omega}{(9\ V - 1.16\ V)} = 6.49\ k\Omega \quad (64)$$

$$R3 = \frac{V_{OVH} - V_{OVL}}{23\ \mu A} = \frac{15\ V - 14\ V}{23\ \mu A} = 43.48\ k\Omega \quad (65)$$

$$R4 = \frac{1.16\ V \times R3}{(V_{OVH} - 1.16\ V)} = \frac{1.16\ V \times 43.48\ k\Omega}{(15\ V - 1.16\ V)} = 3.65\ k\Omega \quad (66)$$

Nearest available 1% resistors should be chosen. Set R1 = 43.2 kΩ, R2 = 6.49 kΩ, R3 = 43.2 kΩ, and R4 = 3.65 kΩ.

9.2.1.2.10 Power Good Pin

When the voltage at the FB pin increases above its threshold, the internal pulldown acting on the PGD pin is disabled allowing PGD to rise to V_{PGD} through the pullup resistor, R_{PG}, as shown in Figure 44. The pullup voltage (V_{PGD}) can be as high as 17 V, and can be higher or lower than the voltages at VIN and OUT. VDD is a convenient choice for V_{PGD} as it allows interface to low voltage logic and avoids glitching on PGD during power-up. If a delay is required at PGD, suggested circuits are shown in Figure 45. In Figure 45A capacitor C_{PG} adds delay to the rising edge, but not to the falling edge. In Figure 45B, the rising edge is delayed by R_{PG1} + R_{PG2} and C_{PG}, while the falling edge is delayed a lesser amount by R_{PG2} and C_{PG}. Adding a diode across R_{PG2} (Figure 45C) allows for equal delays at the two edges, or a short delay at the rising edge and a long delay at the falling edge.

Setting the output threshold for the PGD pin requires two resistors (R4, R5) as shown in Figure 43. While monitoring the output voltage is shown in Figure 43, R4 can be connected to any other voltage which requires monitoring.

The resistor values are calculated as follows:

Choose the upper and lower threshold (V_{PGDH}) and (V_{PGDL}) at V_{OUT}.

$$R4 = \frac{V_{PGDH} - V_{PGDL}}{24\ \mu A} = \frac{V_{PGD(HYS)}}{24\ \mu A}$$

$$R5 = \frac{1.167V \times R4}{(V_{PGDH} - 1.167V)} \quad (67)$$

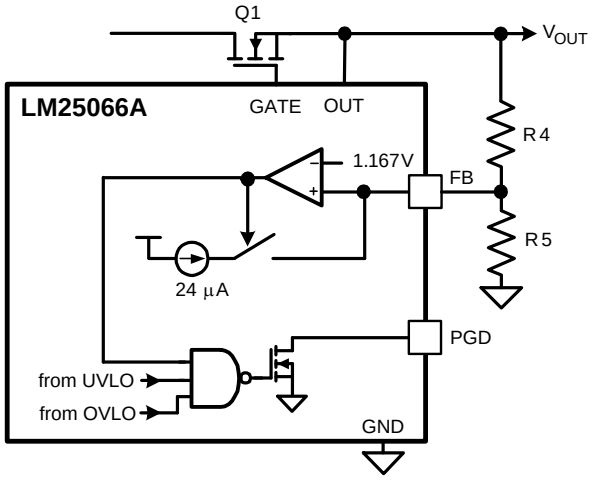


Figure 43. Programming the PGD Threshold

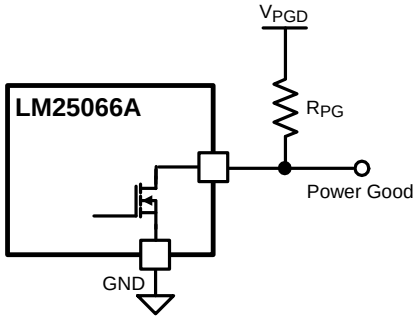


Figure 44. Power Good Output

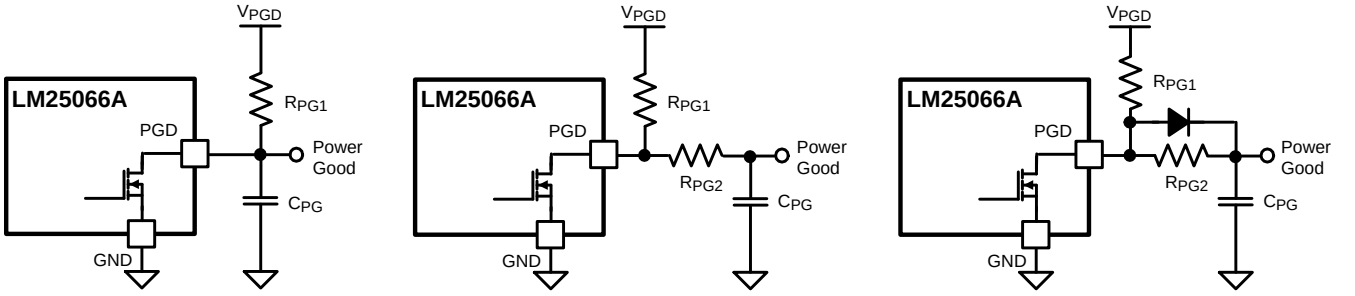


Figure 45. Adding Delay to the Power Good Output Pin

For this example PGDH of 9.25 V and PGDL of 8.75 V is targeted. R5 and R6 are computed using the following equations:

$$R5 = \frac{V_{PGDH} - V_{PGDL}}{24\ \mu A} = \frac{9.25\ V - 8.75\ V}{24\ \mu A} = 10.42\ k\Omega \quad (68)$$

$$R6 = \frac{1.167\ V \times R5}{(V_{PGDH} - 1.167\ V)} = \frac{1.167\ V \times 10.42\ k\Omega}{(9.25\ V - 1.167\ V)} = 1.55\ k\Omega \quad (69)$$

Nearest available 1% resistors should be chosen. Set R5 = 10 kΩ and R6 = 1.5 kΩ.

9.2.1.2.11 Input and Output Protection

Proper operation of the LM25066A hot swap circuit requires a voltage clamping element present on the supply side of the connector into which the hot swap circuit is plugged in. A TVS is ideal, as depicted in Figure 46. The TVS is necessary to absorb the voltage transient generated whenever the hot swap circuit shuts off the load current. This effect is the most severe during a hot-short when a large current is suddenly interrupted when the FET shuts off. The TVS should be chosen to have minimal leakage current at $V_{IN,MAX}$ and to clamp the voltage to under 24 V during hot-short events. For many high power applications, 5.0SMDJ13A is a good choice.

If the load powered by the LM25066A hot swap circuit has inductive characteristics, a Schottky diode is required across the LM25066A's output, along with some load capacitance. The capacitance and the diode are necessary to limit the negative excursion at the OUT pin when the load current is shut off.

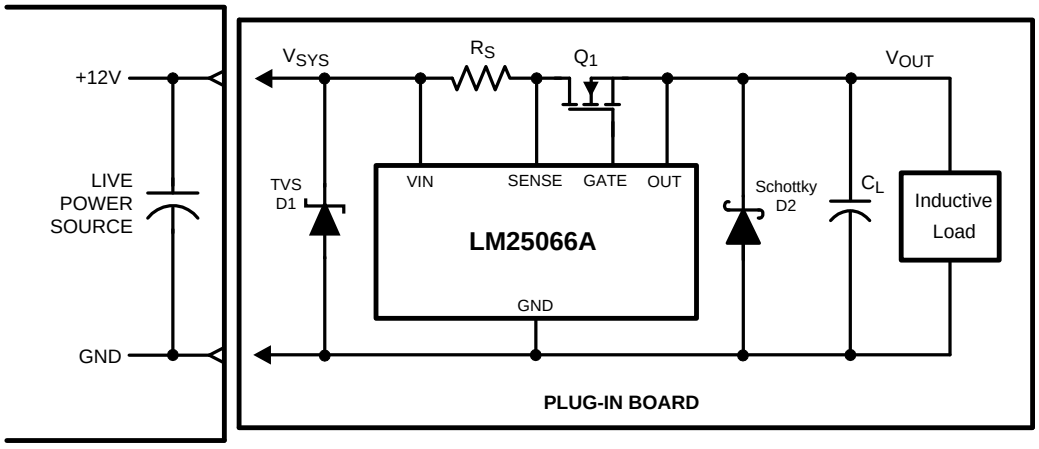


Figure 46. Output Diode Required for Inductive Loads

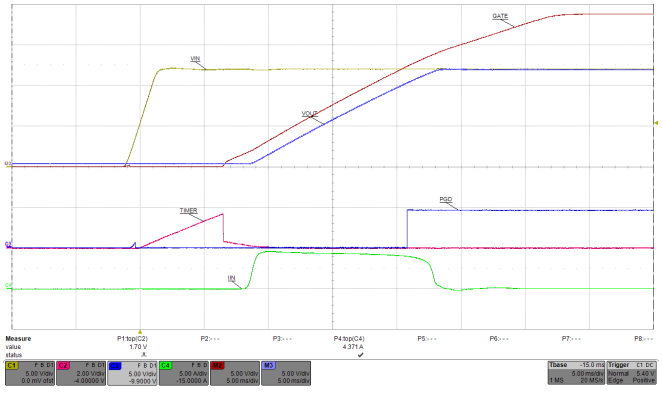
9.2.1.2.12 Final Schematic and Component Values

Figure 38 shows the schematic used to implement the requirements described in the previous section. In addition, Table 45 provides the final component values that were used to meet the design requirements for a 12-V, 45-A hot swap design. Figure 47 to Figure 54 are based on these component values.

Table 45. Final Component Values (12-V, 45-A Design)

COMPONENT	VALUE
R_{SNS}	0.5 mΩ
R1, R3	43.2 kΩ
R2	6.49 kΩ
R4	3.65 kΩ
R_{FB1}	10 kΩ
R_{FB2}	1.5 kΩ
R_{PWR}	5.11 kΩ
Q1	CSD17556Q5B
Q2	MMBT3904
Q3	MMBT3906
D1, D3	1N4148W-7-F
D2	SK153-TP
Z1	5.0MDJA15A
$C_{dV/dt}$	100 nF
C_{TIMER}	22 nF

9.2.2 Application Curves



V_{IN} = 12 V

Figure 47. Start-Up

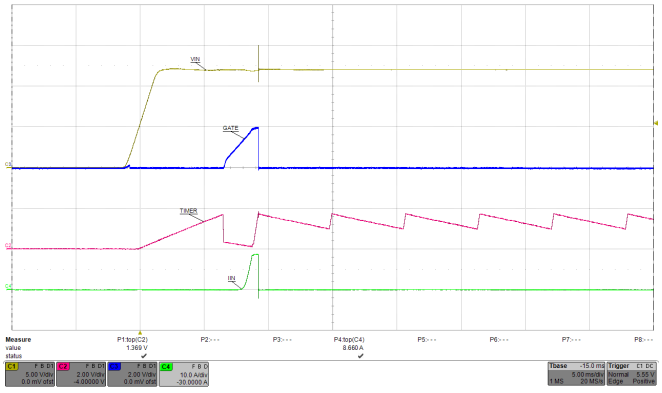


Figure 48. Start-Up into Short

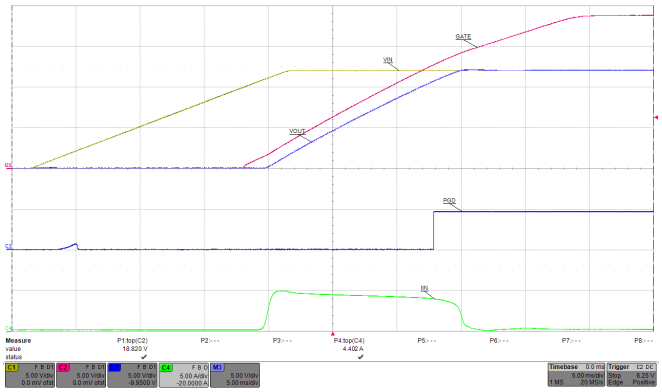


Figure 49. Undervoltage

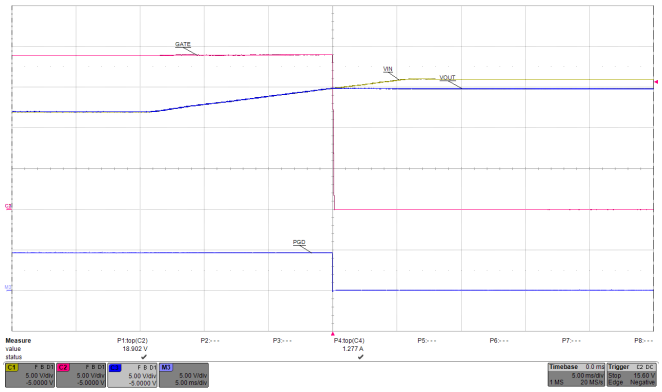


Figure 50. Overvoltage

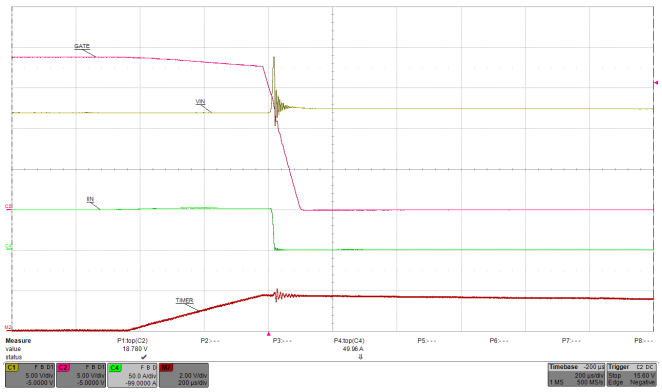


Figure 51. Gradual Overcurrent

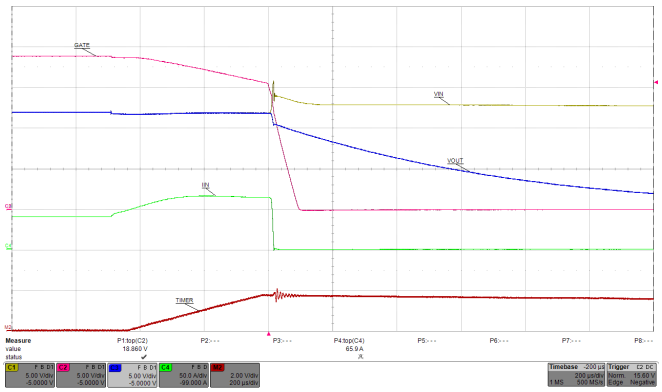


Figure 52. Loadstep

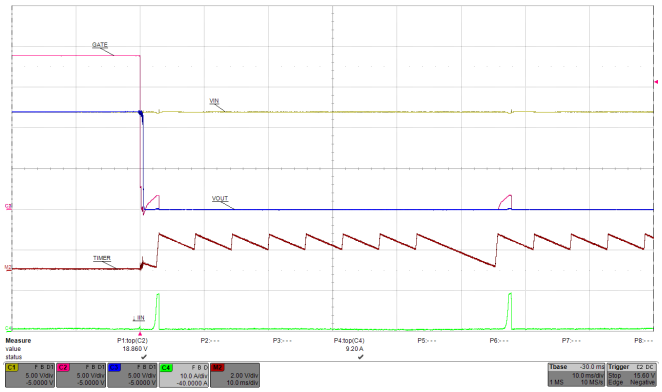


Figure 53. Hot Short on Vout (Zoomed Out)

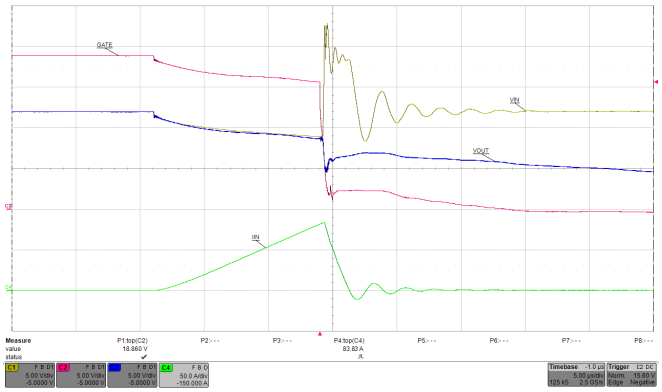


Figure 54. Hotshort on Vout (Zoomed In)

10 Power Supply Recommendations

In general, the LM25066A behavior is more reliable if it is supplied from a very regulated power supply. However, high-frequency transients on a backplane are not uncommon due to adjacent card insertions or faults. If this is expected in the end system, TI recommends to placing a 1-µF ceramic capacitor to ground close to the source of the hot swap MOSFET. This reduces the common mode seen by VIN and SENSE. Additional filtering may be necessary to avoid nuisance trips.

11 Layout

11.1 Layout Guidelines

The following guidelines should be followed when designing the PC board for the LM25066A:

- Place the LM25066A close to the board's input connector to minimize trace inductance from the connector to the MOSFET.
- Note that special care must be taken when placing the bypass capacitor for the VIN pin. During hot shorts, there is a very large dV/dt on input voltage after the MOSFET turns off. If the bypass capacitor is placed right next to the pin and the trace from Rsns to the pin is long, an LC filter is formed. As a result, a large differential voltage can develop between VIN and SENSE. To avoid this, place the bypass capacitor close to Rsns instead of the VIN pin.

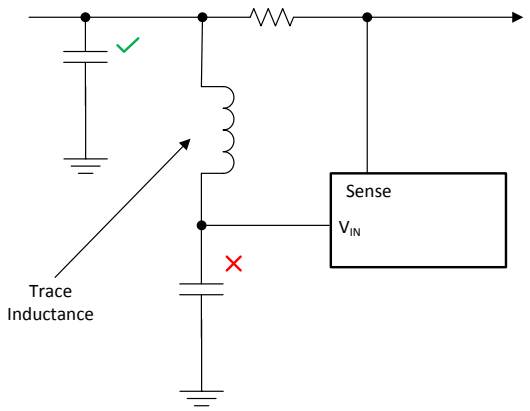


Figure 55. Layout Trace Inductance

- Place a 1-µF capacitor as close as possible to VREF pin.
- Place a 1-µF capacitor as close as possible to VDD pin.
- The sense resistor (R_S) should be placed close to the LM25066A. In particular, the trace to the VIN pin should be made as low resistance as practical to ensure maximum current and power measurement accuracy. Connect R_S using the Kelvin techniques shown in Figure 57.
- The high current path from the board's input to the load (via Q_1) and the return path should be parallel and close to each other to minimize parasitic loop inductance.
- The ground connections for the various components around the LM25066A should be connected directly to each other and to the LM25066A's GND pin and then connected to the system ground at one point, as shown in Figure 58. Do not connect the various component grounds to each other through the high current ground line. For more details, see application note AN-2100.
- Provide adequate heat sinking for the series pass device (Q_1) to help reduce stresses during turnon and turnoff.
- Keep the gate trace from the LM25066A to the pass MOSFET short and direct.
- The board's edge connector can be designed such that the LM25066A detects via the UVLO/EN pin that the board is being removed and responds by turning off the load before the supply voltage is disconnected. For example, in Figure 56, the voltage at the UVLO/EN pin goes to ground before V_{SYS} is removed from the LM25066A because of the shorter edge connector pin. When the board is inserted into the edge connector, the system voltage is applied to the LM25066A's VIN pin before the UVLO voltage is taken high, thereby allowing the LM25066A to turn on the output in a controlled fashion.

11.2 Layout Example

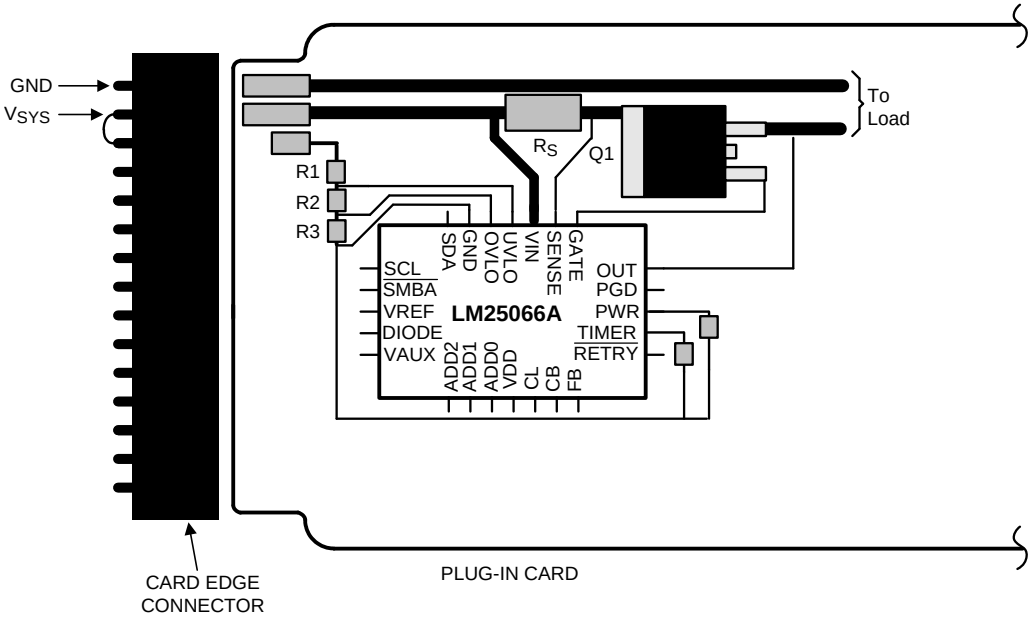


Figure 56. Recommended Board Connector Design

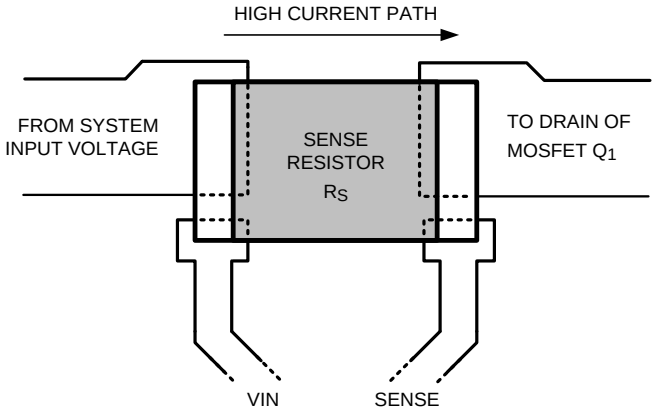


Figure 57. Sense Resistor Connections

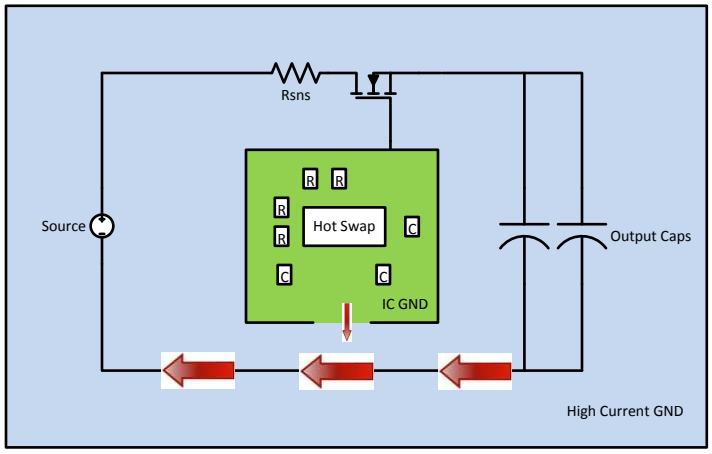


Figure 58. LM25066A Quiet IC Ground Layout

12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

For the LM25066 Design Calculator, go to http://www.ti.com/product/LM25066/toolssoftware.

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM25066APSQ/NOPB	ACTIVE	WQFN	NHZ	24	1000	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	L25066A	Samples
LM25066APSQE/NOPB	ACTIVE	WQFN	NHZ	24	250	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	L25066A	Samples
LM25066APSQX/NOPB	ACTIVE	WQFN	NHZ	24	4500	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	L25066A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

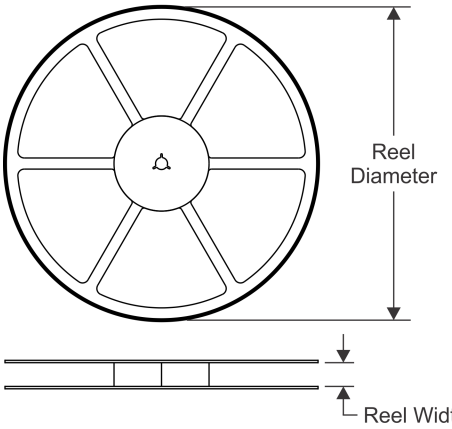
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

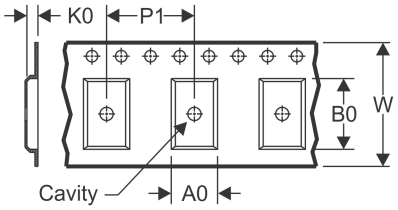
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

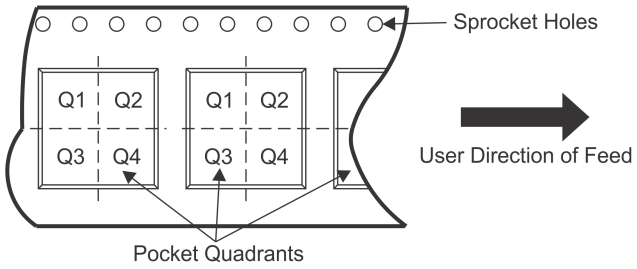


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

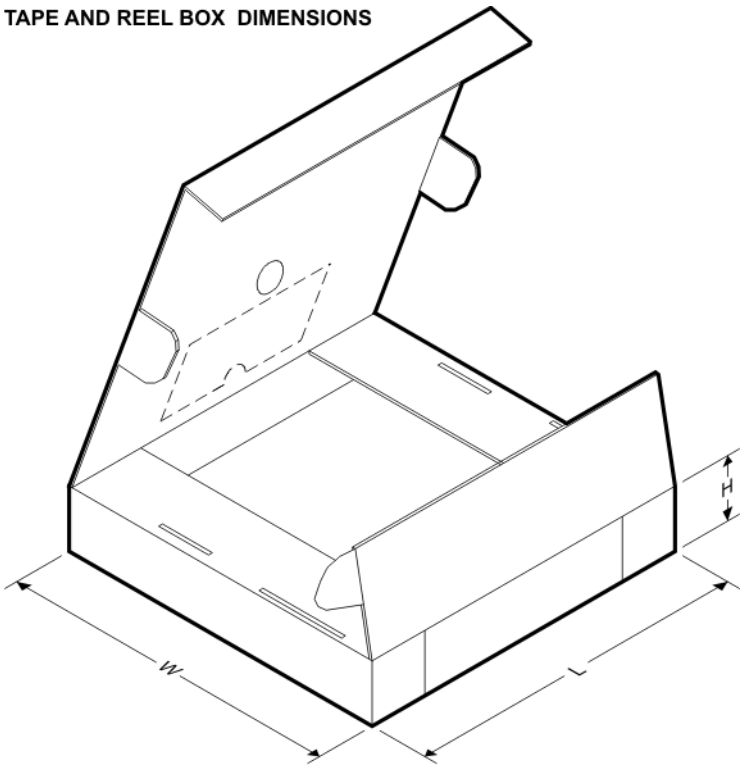
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM25066APSQ/NOPB	WQFN	NHZ	24	1000	178.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1
LM25066APSQE/NOPB	WQFN	NHZ	24	250	178.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1
LM25066APSQX/NOPB	WQFN	NHZ	24	4500	330.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1

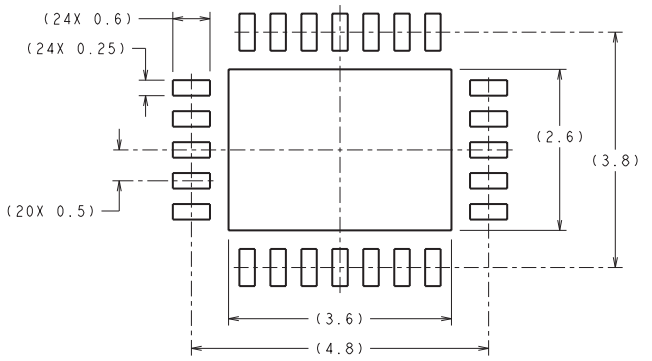
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

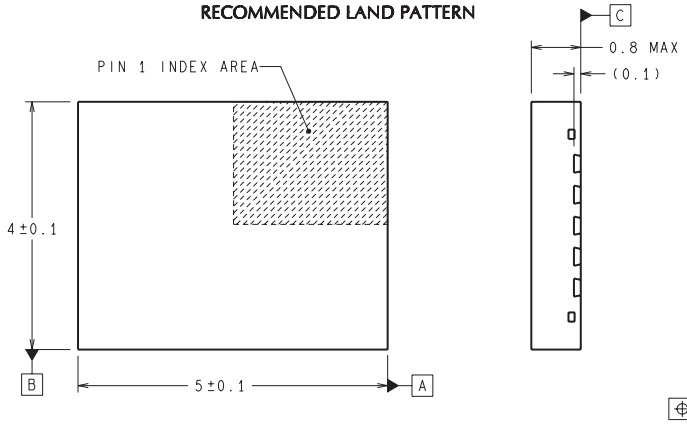
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM25066APSQ/NOPB	WQFN	NHZ	24	1000	208.0	191.0	35.0
LM25066APSQE/NOPB	WQFN	NHZ	24	250	208.0	191.0	35.0
LM25066APSQX/NOPB	WQFN	NHZ	24	4500	356.0	356.0	35.0

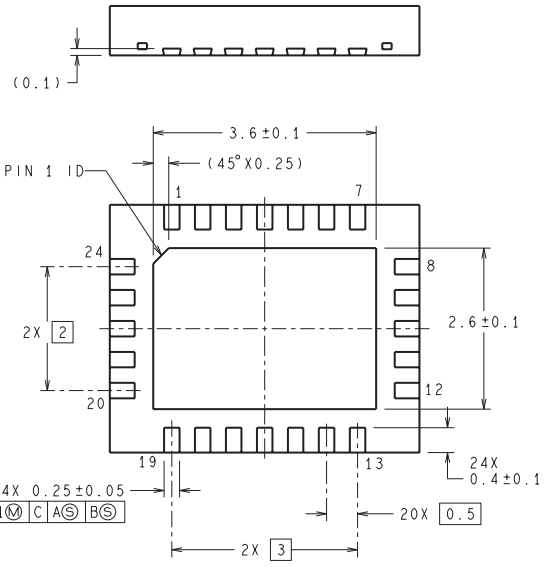
NHZ0024B



RECOMMENDED LAND PATTERN

DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN () FOR REFERENCE ONLY





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